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A New Simple Chaotic Circuit Based on Memristor

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In this paper, a new memristor is proposed, and then an emulator built from off-the-shelf solid state components which imitates the behavior of the proposed memristor is presented. Multisim simulation and breadboard experiment are made on the emulator, exhibiting a pinched hysteresis loop in the voltage-current plane when the emulator is driven by a periodic excitation voltage. In addition, a new simple chaotic circuit is designed by using the proposed memristor and other circuit elements. It is exciting that this circuit with only a linear negative resistor, a capacitor, an inductor and a memristor can generate a chaotic attractor. The dynamical behaviors of the proposed chaotic system are analyzed by Lyapunov exponents, phase portraits and bifurcation diagram. Finally, an electronic circuit is designed to implement the chaotic system. For the sake of simple circuit topology, the proposed chaotic circuit can be easily manufactured at low cost.

Keywords: Memristor; chaotic circuit; Breadboard experiment.

1. Introduction

Memristor as the fourth fundamental circuit element besides resistor, inductor, and capacitor, was first postulated in 1971 by Chua [1971] and later the concept was extended to a kind of dynamical system called generalized memristor in 1976 by Chua and Kang [1976]. Both the memristor and generalized memristor have the common fingerprints of pinched hysteresis loop in the current versus voltage plane under periodic excitation signal condition. The pinched hysteresis loop shrinks as the frequency of excitation signal is increased (the pinched hysteresis loop shrinks to a single-valued function when the frequency of the excitation signal is increased high enough) [Adhikari *et al.*, 2013]. Though the device was postulated theoretically, an actual physical device was not discovered. Until 2008, Strukov and others in HP lab using nanoscale technology first fabricated a physical memristor, which is a two-terminal electrical device based on TiO2 material [Strukov *et al.*, 2008]. Thus the status of memristor as the fourth fundamental circuit element was consolidated. From then on, more and more researchers show great interests in the research of circuits containing memristor. Different application circuits based on memristor were proposed, such as

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memristor-based ReRAM [Seok *et al.*, 2014], memristor-based synapses for neuromorphic circuits [Prezioso *et al.*, 2015], and memristor-based programmable logic circuits [Georgios *et al.*, 2014]. Apart from these, the research of chaotic circuits based on memristor has also become a hot topic. For example, Lin and Wang proposed a new image encryption algorithm based on chaos with PWL memristor in Chua's circuit [Lin and Wang, 2009].

In 2015, the knowm memristor invented by Dr. Kris Campbell in Boise State University is available as a commercial component, which is developed specifically for neuromemristive applications [Dr. Kris Campbell, 2015]. Different from the TiO2 memristor, the knowm memristor is formed by metal W, Ag and Chalcogenide. However, the cost of fabricating knowm memristor is high, and the price is high. Therefore, it is still very necessary to research and design the memristor models and emulators. In order to study the dynamic behaviors of memristive circuit, a lot of memristor models were proposed. For example, piecewise linear models [Itoh and Chua, 2008; Muthuswamy and Kokate, 2009], and SPICE macromodels [Benderli and Wey, 2009; Rak and Cserey, 2010; Batas and Fiedler, 2011] were proposed to emulate the memristor's behaviors. Although those models are useful for simulating memristor, they can not be used to physically build real-world application circuits based on memristor. Therefore, designing a memristor emulator would be very useful for experimentally exploring the dynamic behaviors of memristive circuit. In 1971, Chua proposed the first memristor emulator based on active devices [Chua, 1971]. However, this emulator circuit is relatively complex and bulky. After that, Pershin and Ventra proposed another emulator, which based on microcontroller [Pershin and Ventra, 2010]. Nonetheless, the frequency range of this emulator circuit is limited to approximately 50 Hz. Besides, a smooth continuous nonlinear memristor emulator formed by operational amplifiers (Op Amps) and analog multipliers was proposed by Muthuswamy [2010a], which has frequency content in the 0.5 kHz range. Recently, Yang proposed a HP memristor emulator that contains most of features of a real memristor, such as a sufficiently wide range of memristance, bimodal operability of pulse and continuous signal inputs, a long period of nonvolatility, floating operation, operability with other devices, and the ability to be implemented with off-the-shelf devices. Specifically, the proposed emulator has a wide memristance range [Yang *et al.*, 2015]. However, when the frequency of the sinusoidal input applied to this emulator is equal to 1kHz, the pinched hysteresis loop of this emulator shrinks to a single-valued function, which means this emulator's operation frequency is no larger than 1kHz.

In this paper, a new memristor is proposed and an emulator is also presented. Different from these piecewise linear memristors proposed by Muthuswamy and Kokate [2009] and Itoh and Chua [2008], our proposed memristor is a smooth continuous nonlinearity memristor, which makes the physical realization of this memristor easy. Meanwhile, the memristor's memductance function only contains a quadratic nonlinearity term without constant term, which can make the memristor's mathematical model simpler compared with above mentioned smooth continuous nonlinear memristor [Muthuswamy, 2010a]. And unlike the emulator circuit proposed by Muthuswamy [2010a] who use the Op-amp AD711KN to realize the current-inverter, we use the current feedback operational amplifier AD844 to realize the current-inverter, which makes the design of emulator more easy. Compared to the recent memristor emulator proposed by Yang [Yang *et al.*, 2015], which is a completed current (or charge)-controlled memristor emulator based on the HP memristor mathematical model, our realized memristor emulator is a generalized voltage-controlled memristor emulator based on the proposed new memristor mathematical model. According to the simulation and experimental results we confirm our proposed emulator still can show a pinched hysteresis loop when the frequency of the sinusoidal input applied to the emulator is equal to 1.5kHz, so the emulator's operation frequency is larger than 1.5kHz, which shows a higher frequency range than the microcontroller emulator proposed by Pershin and Ventra [2010], the above mentioned smooth continuous nonlinear emulator proposed by Muthuswamy [2010a] and the emulator proposed by Yang [Yang *et al.*, 2015].

In addition, due to the nonlinearity of memristor, memristor-based circuits can easily generate a chaotic signal [Bao *et al.*, 2011a]. Using memristor to construct chaotic system has attracted a lot of interest. More and more chaotic circuits based on memristor were proposed [Barboza and Chua, 2008; Muthuswamy and Kokate, 2009; Li *et al.*, 2009; Wang *et al.*, 2009; Muthuswamy and Chua, 2010b; Muthuswamy, 2010a; Bao *et al.*, 2011a,b; Hrubos *et al.*, 2012; Wang *et al.*, 2012; Buscarino *et al.*, 2012a,b; Itoh *et al.*, 2013; Setoudeh *et al.*, 2014; Li *et al.*, 2014] since the first memristor-based chaotic circuit was proposed by Itoh and Chua in 2008 [Itoh and Chua, 2008]. A variety of chaotic circuits based on HP memristor were proposed [Li *et al.*, 2014; Wang *et al.*, 2012; Buscarino *et al.*, 2012a,b; Setoudeh *et al.*, 2014]. For example, Buscarino *et al.* [2012b] proposed a memristor-based chaotic circuit by making use of two HP memristors in antiparallel to substitute the Chua's diode in the canonical Chua's oscillator. However, the above proposed chaotic systems based on HP memristor only made computer verification and didn't make experimental verification. Besides, chaotic circuits based on piecewise-linear memristor were proposed [Muthuswamy and Kokate, 2009; Itoh *et al.*, 2013; Li *et al.*, 2009; Wang *et al.*, 2009]. For example, Muthuswamy and Kokate [2009] proposed memristor-based chaotic circuits with the memductance mathematically defined as piecewise linear discontinuous function $W(\varphi) = dq(\varphi)/d\varphi$. These memristor-based chaotic circuits can generate various chaotic attractors. However, the constitutive relations of these memristors are nonsmooth piecewise linear functions, resulting in discontinuous nonlinear characteristics of the memristance $M(\varphi)$ and memductance $W(\varphi)$, which makes the physical realization of such nonsmooth memristors impossible [Bao *et al.*, 2011a]. Chaotic circuits based on smooth continuous nonlinearity memristor were proposed [Bao *et al.*, 2011a; Muthuswamy, 2010a; Bao *et al.*, 2011b; Hrubos *et al.*, 2012; Muthuswamy and Chua, 2010b]. For example, Bao designed a simple memristor-based chaotic circuit using a negative inductor, a negative resistor and a negative capacitor in series with a parallel combination of a memristor and a capacitor [Bao *et al.*, 2011a].

By using the memristor proposed in this paper, we designed a new simple memristor-based chaotic circuit. The memristor-based chaotic circuit consists of an inductor and a negative resistor in series with a parallel combination of a memristor and a capacitor, which is simpler compared to those memristor-based chaotic circuits reported in above mentioned papers. Compared to circuit in paper [Bao *et al.*, 2011a], our proposed memristor-based chaotic circuit requires only one negative element, which is advantageous because it reduces the number of active elements and reduces power consumption accordingly.

This paper is organized as follows. In Sect. 2, some fundamentals of memristor are illustrated, a new memristor is proposed, and an emulator built from off-the-shelf solid state components which imitates the behavior of the proposed memristor is presented. In Sect.3, the memristor-based chaotic circuit topology, system equations are described and then the dynamics of chaos are confirmed by numerical computation. In Sect. 4, an electronic circuit is designed to implement the chaotic system. Finally, conclusions are given in Sect. 5.

2. The Memristor and Emulator

According to Chua and Kang [1976], a generalized memristor is defined by

$$\begin{cases} y = g(z,u)u \\ \dot{z} = f(z,u) \end{cases} \tag{1}$$

where u and y denote the input and output of the system respectively, z denotes the state of the system. The g is a continuous n-dimensional vector function and f is a continuous scalar function. The output y is zero whenever the input u is zero, regardless of the state z which incorporates the memory effect. This property manifests that the pinched hysteresis loop always passes through the origin. A generalized current-controlled memristor is defined by

$$\begin{cases} v = M(z_1, z_2, \cdots, z_n)i \\ \dot{z}_k = f_k(z_1, z_2, \cdots, z_n; i), k = 1, 2, \cdots n \end{cases} \tag{2}$$

where M called as the memristance is a continuous function of $z_1, z_1, \cdots, z_n$, and $z_1, z_1, \cdots, z_n$ are the state variables defined by n-order system of differential equations. Alternatively, a generalized voltage-controlled memristor is defined by

$$\begin{cases} i = W(z_1, z_2, \cdots, z_n)v \\ \dot{z}_k = f_k(z_1, z_2, \cdots, z_n; v), k = 1, 2, \cdots n \end{cases} \tag{3}$$

where W called as the memductance is a continuous function of the state variables $z_1, z_1, \cdots, z_n$.

Now, we define a generalized voltage-controlled memristor as

$$\begin{cases} i = \alpha z^2 v \\ \dot{z} = -\beta v - \lambda z + \kappa v z \end{cases} \tag{4}$$

where $\alpha, \beta, \lambda, \kappa$ are parameters and $\alpha > 0$ (the intention for this choice is to keep the memristor a passive one). z is the internal state of the memristor. Compared with those memristors proposed by Muthuswamy [2010a] and Bao [Bao *et al.*, 2011a], the proposed memristor's memductance $W = \alpha z^2$ only contains a quadratic nonlinearity term and does not contain constant term. The intention is to make the mathematical model simpler and its emulator easier to be implemented.

Now, an emulator built from off-the-shelf solid state components which imitates the behavior of the above proposed memristor is designed, as shown in Fig.1.

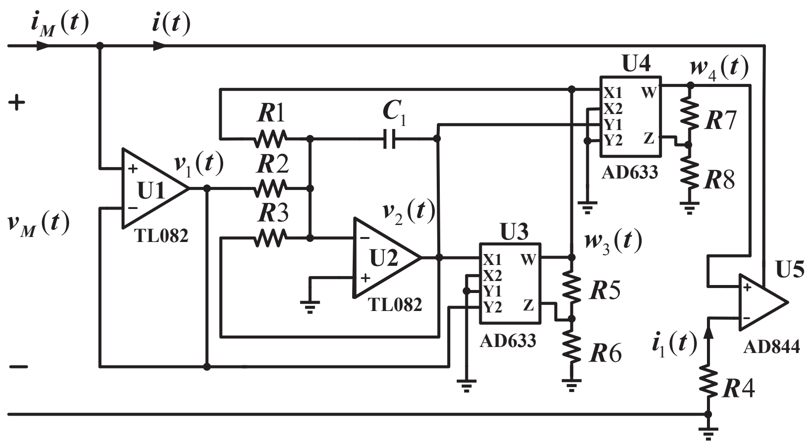

Fig. 1. Schematic of the emulator.

With the properties of Op-amp TL082, multiplier AD633 and current feedback operational amplifier AD844 (refer to the datasheet for further information), we can see that U5 is the current-inverter that implements

$$i_M(t) = i(t) = i_1(t) = -\frac{w_4(t)}{R_4} \tag{5}$$

Multiplier U3 implements

$$w_3(t) = -\frac{(R_5 + R_6)}{10R_5} v_2(t) \cdot v_1(t) \tag{6}$$

Multiplier U4 implements

$$w_4(t) = \frac{(R_7 + R_8)}{10R_7} w_3(t) \cdot v_2(t) \tag{7}$$

Op-amp U1 implements

$$v_1(t) = v_M(t) \tag{8}$$

Op-amp U2 implements

$$\frac{dv_2(t)}{dt} = -\frac{w_3(t)}{R_1C_1} - \frac{v_1(t)}{R_2C_1} - \frac{v_2(t)}{R_3C_1} \tag{9}$$

Substituting for w_3 from Eq.(6) into Eq.(7) and then substituting w_4 into Eq.(5) we can get following Eq.(10) after simplification

$$i_M(t) = \frac{(R_5 + R_6)(R_7 + R_8)}{100R_4R_5R_7} v_2(t)^2 \cdot v_1(t) \tag{10}$$

Substituting for v_1 from Eq.(8) into Eq.(10) we can get

$$i_M(t) = \frac{(R_5 + R_6)(R_7 + R_8)}{100R_4R_5R_7} v_2(t)^2 \cdot v_M(t) \tag{11}$$

Finally, substituting for w_3 and v_1 from Eq.(6) and Eq.(8) into Eq.(9) we can get the following differential equation governing the internal state of the emulator

$$\frac{dv_2(t)}{dt} = -\frac{v_M(t)}{R_2C_1} - \frac{v_2(t)}{R_3C_1} + \frac{(R_5+R_6)v_M(t)\cdot v_2(t)}{10R_1R_5C_1} \tag{12}$$

Along with the above function Eq.(11) and Eq.(12) we have

$$\begin{cases} i_M(t) = \frac{(R_5+R_6)(R_7+R_8)}{100R_4R_5R_7}v_2(t)^2\cdot v_M(t) \\ \frac{dv_2(t)}{dt} = -\frac{v_M(t)}{R_2C_1} - \frac{v_2(t)}{R_3C_1} + \frac{(R_5+R_6)v_M(t)\cdot v_2(t)}{10R_1R_5C_1} \end{cases} \tag{13}$$

Now, we consider the above proposed memristor defined by Eq.(4). Comparing Eq. (13) with Eq.(4), and making $i = i_M(t)$, $v = v_M(t)$, $z = v_2(t)$(the internal state of the memristor), $\alpha = \frac{(R_5+R_6)(R_7+R_8)}{100R_4R_5R_7}$, $\beta = \frac{1}{R_2C_1}$, $\lambda = \frac{1}{R_3C_1}$, $\kappa = \frac{(R_5+R_6)}{10R_1R_5C_1}$, we can see that Fig.1 indeed realize the above proposed memristor. And unlike Muthuswamy [2010a] who used the Op-amp AD711KN to realize the current-inverter, we use the current feedback operational amplifier AD844 to realize the current-inverter, which makes the design more easy.

When making $R_1 = R_4 = 10K\Omega, R_2 = R_3 = 25K\Omega, R_5 = R_7 = 1K\Omega, C_1 = 300nF$, $R_6 = R_8 = 9K\Omega$, we can obtain the experimental results of the $i_M - v_M$ characteristics, as shown in Fig. 2(c) and (d), which are entirely consistent with the results obtained by Multisim simulation shown in Fig. 2(a) and (b). From the simulation and experimental results we can know our proposed emulator shows a higher frequency range than the microcontroller emulator proposed by Pershin and Ventra [2010], the smooth continuous nonlinear emulator proposed by Muthuswamy [2010a] and the emulator proposed by Yang [Yang *et al.*, 2015]. From Eq.(5) we know that $i_M(t) = -w_4(t)/R_4$. In order to conveniently measure the current i_M we use the voltage w_4 to substitute the current i_M, which just makes a transformation of $-1/R_4$ scale.

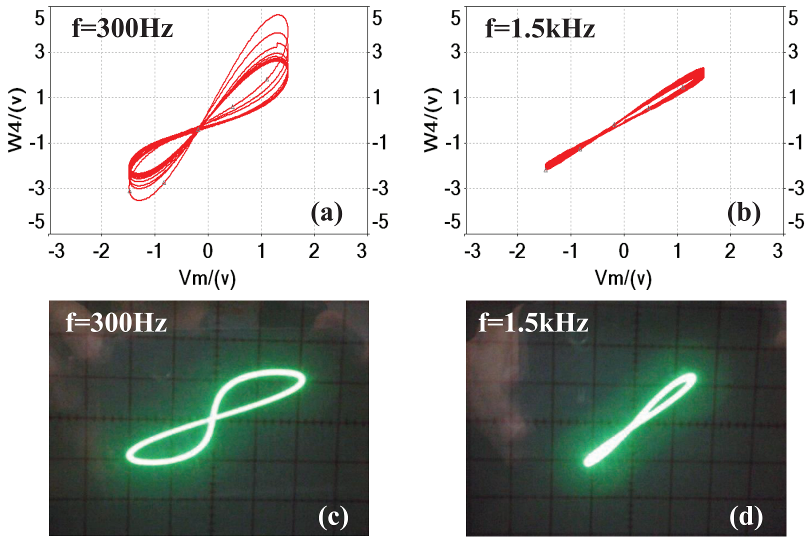

Fig. 2. The $i_M - v_M$ characteristics of memristor, the excitation signal is a sinusoid voltage with 1.5V amplitude, (a) and (b) are the Multisim simulation results with a frequency of 300Hz and 1.5kHz respectively, the scales are 2.0V /div for w_4 and 1.0V/div for v_M, (c) and (d) are the corresponding experimental results.

3. Chaotic System

In this section, the chaotic circuit topology, system equations and dynamical characteristics including bifurcation diagram, Lyapunov exponent spectrum, equilibrium points and eigenvalues are described.

3.1. *Circuit topology and system equations*

By adding an inductor, a capacitor, a linear negative resistor to the above proposed memristor, a new chaotic circuit is designed, as shown in Fig.3.

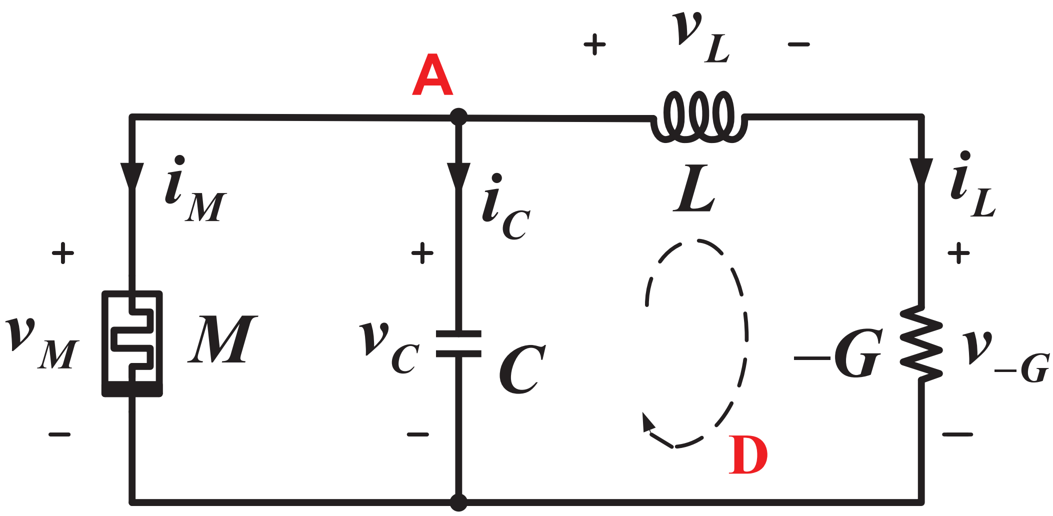

Fig. 3. Schematic of the proposed chaotic system.

Based on Fig. 3, we can see that $v_M = v_C$. By applying Kirchhoff's voltage law to the loop D and using the constitutive relations of the inductor, capacitor and linear negative resistor, we can get the following equations

$$\begin{aligned} & v_L + v_{-G} - v_C = 0 \\ & \Rightarrow L\tfrac{di_L}{dt} = -v_{-G} + v_C \\ & \Rightarrow \tfrac{di_L}{dt} = \tfrac{1}{L}(-v_{-G} + v_C) \\ & \Rightarrow \tfrac{di_L}{dt} = \tfrac{1}{L}(G \cdot i_L + v_C) \end{aligned} \tag{14}$$

By applying Kirchhoff's current law to the node A and using the constitutive relations of the inductor, capacitor, memristor and linear negative resistor, we can get the following equations

$$\begin{aligned} & i_C + i_M + i_L = 0 \\ & \Rightarrow C\tfrac{dv_C}{dt} = -i_L - i_M \\ & \Rightarrow \tfrac{dv_C}{dt} = \tfrac{1}{C}(-i_L - i_M) \\ & \Rightarrow \tfrac{dv_C}{dt} = \tfrac{1}{C}(-i_L - \alpha \cdot z^2 \cdot v_M) \\ & \Rightarrow \tfrac{dv_C}{dt} = \tfrac{1}{C}(-i_L - \alpha \cdot z^2 \cdot v_C) \end{aligned} \tag{15}$$

Finally, according to Eq.(4) we get the equation governing the internal state of the memristor as follows

$$\frac{dz}{dt} = -\beta \cdot v_M - \lambda \cdot z + \kappa \cdot v_M \cdot z \tag{16}$$

Substituting $v_M = v_C$ into Eq.(16) we can get the following equation

$$\frac{dz}{dt} = -\beta \cdot v_C - \lambda \cdot z + \kappa \cdot v_C \cdot z \tag{17}$$

By jointing Eq.(14), Eq.(15), and Eq.(17) , a set of three first-order differential equations defining the relation among the three variables are obtained

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}(G \cdot i_L + v_C) \\ \frac{dv_C}{dt} = \frac{1}{C}(-i_L - \alpha \cdot v_C \cdot z^2) \\ \frac{dz}{dt} = -\beta \cdot v_C - \lambda \cdot z + \kappa \cdot v_C \cdot z \end{cases} \tag{18}$$

We have $x(t) \triangleq i_L$(current through inductor L) and $y(t) \triangleq v_C$ (voltage across capacitor C). The parameter values are $L = 1$, $C = 3$, $G = 0.2$, $\alpha = \kappa$=1, $\beta = \lambda = 0.4$. The above circuit equations can be described as

$$\begin{cases} \dot{x} = 0.2x + y \\ \dot{y} = -\frac{1}{3}x - \frac{1}{3}yz^2 \\ \dot{z} = -0.4y - 0.4z + yz \end{cases} \tag{19}$$

The phase portraits of system (19) are investigated by numerical simulation with initial condition $x(0) = y(0) = z(0) = 0.1$, as shown in Fig. 4. The projections of phase portrait on $x - y$, $x - z$, $y - z$ planes are shown in Fig. 4(a)-(c), respectively. The 3-D view in the $x - y - z$ space is shown in Fig. 4(d). From the numerical simulation results we can know system(19) can generate a chaotic attractor.

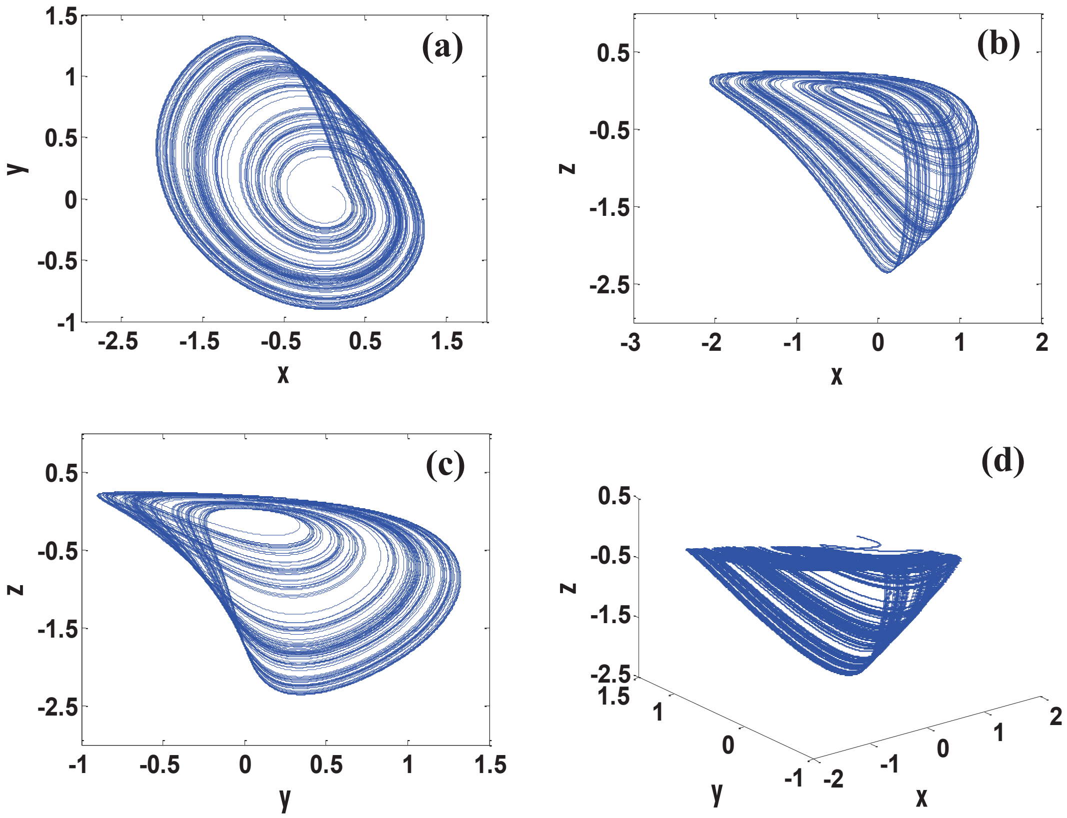

Fig. 4. Chaotic phase portraits of system (19). (a) Projection on $x - y$ plane. (b) Projection on $x - z$ plane. (c) Projection on $y - z$ plane. (d) 3-D view in the $x - y - z$ space.

3.2. *Lyapunov exponents and bifurcation diagram*

Lyapunov exponents provide empirical evidence of chaotic behavior. They characterize the rate of separation of infinitesimally close trajectories in state space [Eckmann and Ruelle, 1985; Wolf *et al.*, 1985]. The rate of separation can be different for different orientations of the initial separation vector, hence the number of Lyapunov exponents is equal to the number of dimensions in phase space. So for a three dimensional autonomous continuous time system, we will have three Lyapunov exponents. A positive Lyapunov exponent implies that the trajectory of a system expands in phase space. However, if the sum of Lyapunov exponents is negative, then the trajectory of the system contracts a little volume in phase space. These two seemingly contradictory properties indicate chaotic behavior in a dynamical system.

To explore the dynamic behaviors of the memristor-based chaotic circuit, the Lyapunov spectrum of system (18) is calculated, as shown in Fig.5 (a). (with the parameter values L=1, C=3, G=0.2, $\alpha = \kappa$=1,

$\beta = 0.4$ and $\lambda = 0 \sim 1$). Notice that when $\lambda = 0.4$, the corresponding Lyapunov exponents are: $LE_1 = 0.046, LE_2 = 0, LE_3 = -0.397$. There is a positive Lyapunov exponent and the sum of the Lyapunov exponent is negative, which indicate chaotic behavior of system (18). Fig.5 (b) shows the bifurcation diagram of system (18) with the parameter values L=1, C=3, G=0.2, $\alpha = \kappa$=1, $\beta = 0.4$ and $\lambda = 0 \sim 1$. It can be observed that system (18) evolves into chaos through double-period bifurcation route.

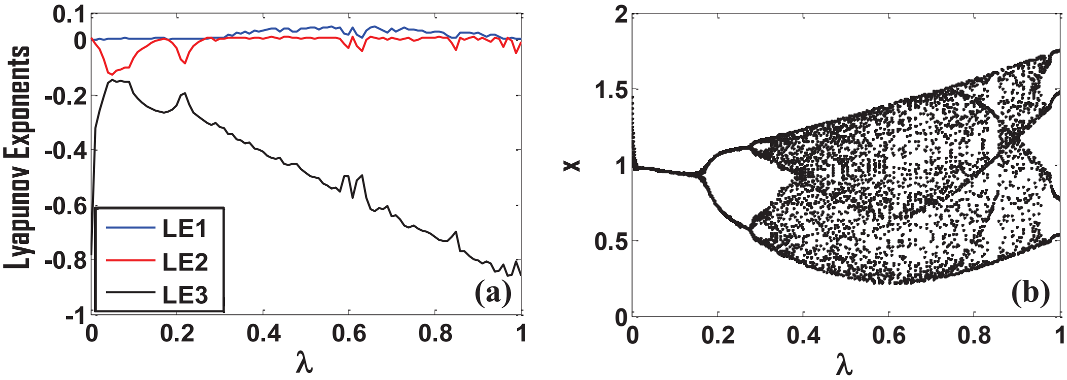

Fig. 5. (a) Lyapunov exponents versus parameter λ of system (18). (b) Bifurcation diagram for increasing parameter λ of system (18).

3.3. *Equilibrium points and stability analysis*

According to system (19), let $\dot{x} = \dot{y} = \dot{z} = 0$, the equilibrium point equations can be expressed as

$$\begin{cases} 0.2x + y = 0 \\ -\frac{1}{3}x - \frac{1}{3}yz^2 = 0 \\ -0.4y - 0.4z + yz = 0 \end{cases} \tag{20}$$

By solving Eq.(20) we get three equilibrium points $S_0 = (0, 0, 0)^T$, $S_1 = (-2.4357, 0.4871, 2.2361)^T$, $S_2 = (-1.6965, 0.3393, -2.2361)^T$. The stability of equilibrium point can be judged by the eigenvalues of the characteristic equation $\det(\lambda I - J) = 0$. Jacobian matrix of system (19) is shown in Eq.(21)

$$J = \begin{bmatrix} 0.2 & 1 & 0 \\ -\frac{1}{3} & -\frac{1}{3}z^2 & -\frac{2}{3}yz \\ 0 & -0.4 + z & -0.4 + y \end{bmatrix} \tag{21}$$

For equilibrium point S_0, the characteristic equation is as follows,

$$\det(\lambda I - J) = \begin{vmatrix} \lambda - 0.2 & -1 & 0 \\ \frac{1}{3} & \lambda & 0 \\ 0 & 0.4 & \lambda + 0.4 \end{vmatrix} = \lambda^3 + 0.2\lambda^2 + 0.2533\lambda + 0.1333 = 0 \tag{22}$$

The solutions (also called as eigenvalues) of above equation are $\lambda_{1,2} = 0.1 \pm 0.5686i$, $\lambda_3 = -0.4$. The stability of system (19) near the equilibrium point S_0 is uniquely determined by these eigenvalues. From the solutions, we know there are one real eigenvalue and a pair of complex conjugate eigenvalues (a so-called index-2 saddle-focus), which are the criteria to generate chaotic attractor. Similarly, the stability of system (19) near the equilibrium points S_1 and S_2 are determined by the eigenvalues $\lambda_{1,2} = -0.7796 \pm 0.9368i$, $\lambda_3 = 0.1795$ (a so-called index-1 saddle-focus) and the eigenvalues $\lambda_{1,2} = -0.8427 \pm 0.9892i$, $\lambda_3 = 0.1579$ (a so-called index-1 saddle-focus) respectively. From the equilibrium point analysis, we know the system (19) contains one index-2 saddle-focus (the premise to generate chaotic attractor) and two index-1 saddle-focus, which provide the possibility to generate chaotic attractor [Yu *et al.*, 2011].

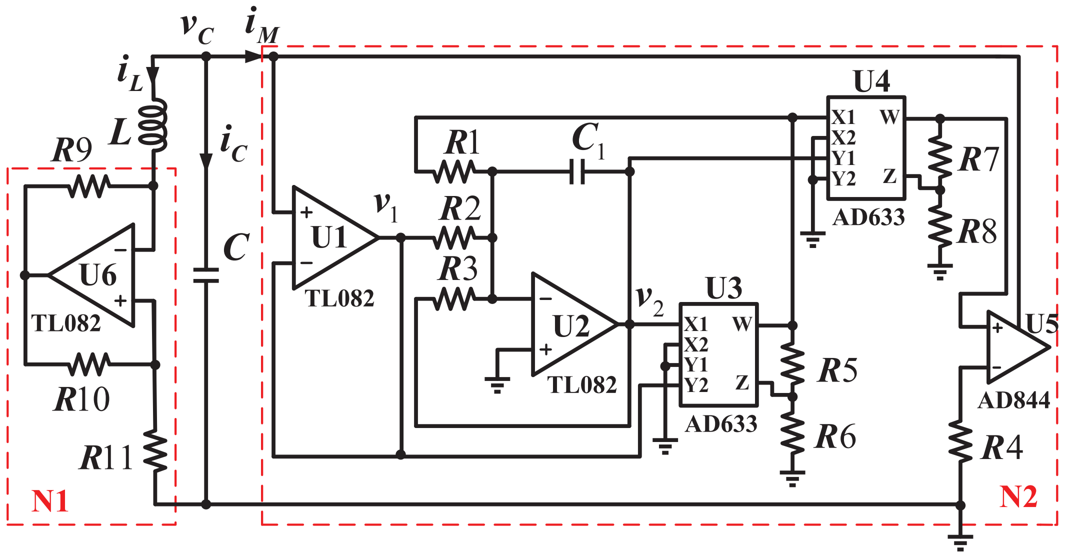

Fig. 6. The schematic of the chaotic circuit based on memristor. The power supplies for the ICs are $\pm 15V$. The circuit in the N1 is a linear negative resistor and N2 is the proposed memristor.

4. Circuit Implementation

In this section, the system (19) is realized by an electronic circuit, as shown in Fig. 6.

The corresponding circuit equations can be described as

$$\begin{cases} \frac{di_L}{dt} = \frac{1}{L}(v_C + \frac{R_9R_{11}}{R_{10}} \cdot i_L) \\ \frac{dv_C}{dt} = \frac{1}{C}(-i_L - \frac{(R_5+R_6)(R_7+R_8)}{100R_4R_5R_7} \cdot v_C \cdot {v_2}^2) \\ \frac{dv_2}{dt} = -\frac{v_C}{R_2C_1} - \frac{v_2}{R_3C_1} + \frac{(R_5+R_6)}{10R_1R_5C_1} \cdot v_C \cdot v_2 \end{cases} \tag{23}$$

where $G = (R_9R_{11})/R_{10}$, $\alpha = (R_5 + R_6)(R_7 + R_8)/(100R_4R_5R_7)$, $\beta = 1/(R_2C_1)$, $\lambda = 1/(R_3C_1)$, $\kappa = (R_5 + R_6)/(10R_1R_5C_1)$. Thus in order to get the parameter values $L = 1$, $C = 3$, $G = 0.2$, $\alpha = \kappa = 1$, $\beta = \lambda = 0.4$, we set $R_9 = 200\Omega$, $R_{10} = 100K\Omega$, $R_{11} = 100\Omega$, $R_4 = R_5 = R_7 = 100\Omega$, $R_6 = R_8 = 9.9K\Omega$, $R_2 = R_3 = 25K\Omega$, $R_1 = 100K\Omega$, $C_1 = 100uF$, $C = 3F$, $L = 1H$. The experimental results of Fig.6 are shown in Fig.8 (a), (b), (c) and (d), which are entirely consistent with the results obtained by Multisim simulation shown in Fig.7 (a), (b), (c) and (d).

5. Conclusions

In this paper, in order to design and realize a simple memristor-based chaotic circuit, a memristor with simple mathematical model is proposed, and then its emulator is also presented. By adding an inductor, a capacitor, and a linear negative resistor to the proposed memristor, a new simple chaotic circuit is proposed. The new constructed system can generate a attractor with the unusual feature of having three equilibrium points, which is unlike the reported memristive systems having a line of equilibrium points. Some basic properties of the new system are investigated including phase portraits, equilibrium, Lyapunov exponent spectrum and bifurcation diagram. Moreover, a practical equivalent circuit of the memristor is presented. Based on the equivalent circuit of memristor, the new chaotic circuit can be easily designed, and the experiment results of chaotic circuit are entirely consistent with the simulation results. Theoretical analysis, numerical simulation and experimental results have confirmed the effectiveness of this approach.

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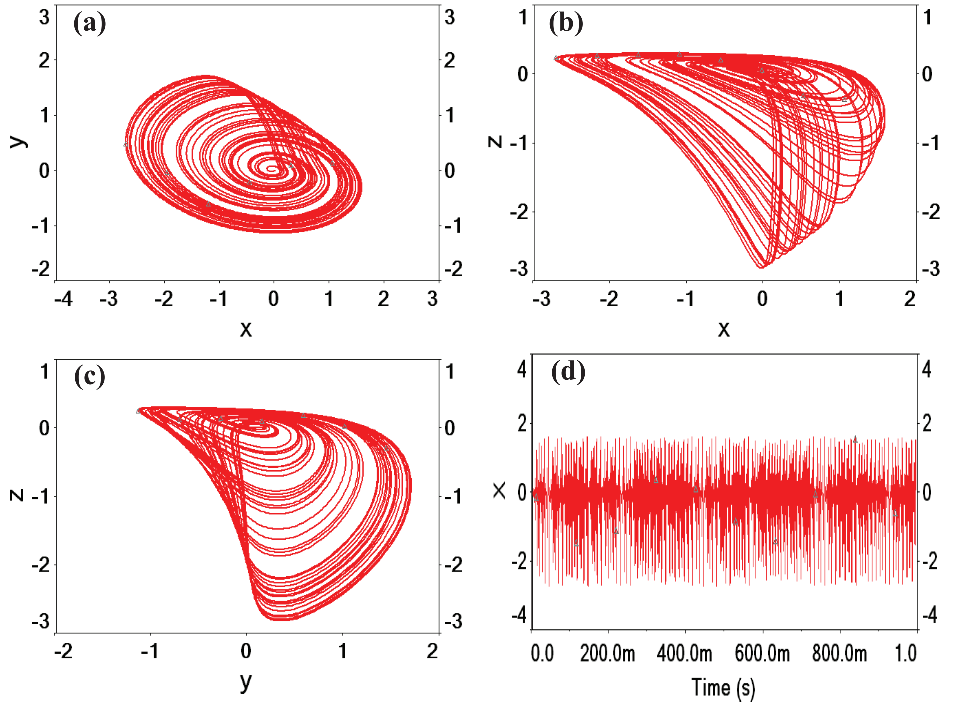

Fig. 7. Phase portraits of system (19) obtained by Multisim simulation. (a) x-y plane. (b) x-z plane. (c) y-z plane. (d) Time-domain waveform of x.

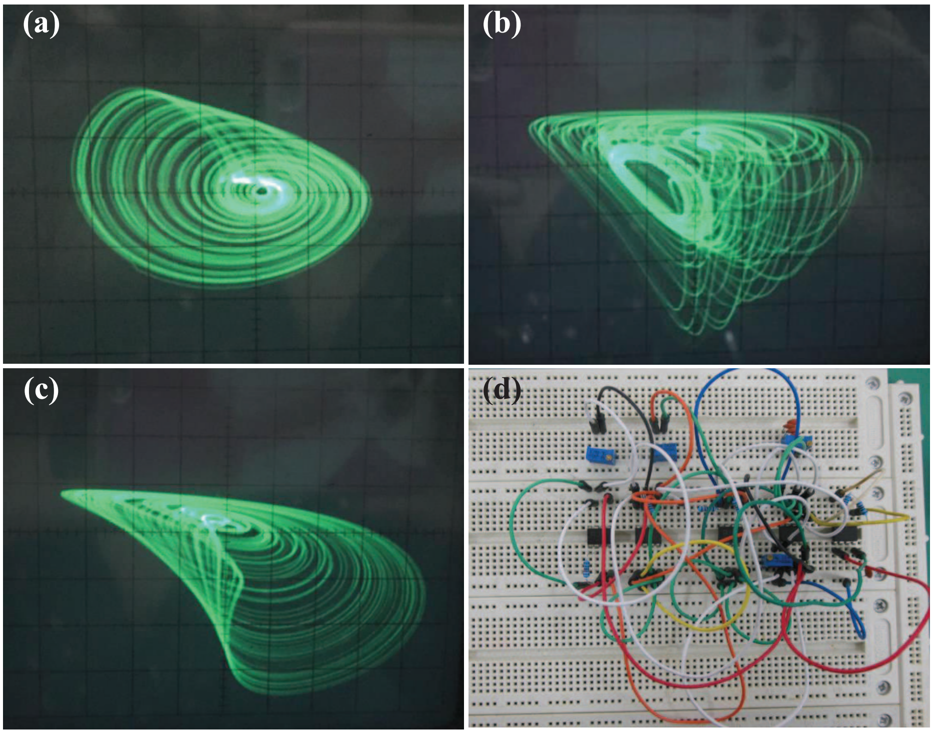

Fig. 8. Phase portraits of system (19) observed from oscilloscope. (a) x-y plane. (b) x-z plane. (c) y-z plane. (d) The physical implementation of circuit.

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