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A Low Power High Gain CMOS LNA with Multiple-Feedback Network for Low Voltage UWB Receiver*

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In this paper, a high gain low voltage low power Complementary Metal Oxide Semiconductor (CMOS) Low-noise Amplifier (LNA) using Chartered 0.18 μm CMOS process for Ultra-wideband (UWB) receiver applications is presented. A novel multiple-feedback network constructed by the shunt feedback resistor with a transformer is adopted to realize desirable bandwidth extension and less chip area occupation in the common-source stage. All the cascaded transistors are configured by current-reuse structure and adjusted by forward body bias technique to further reduce supply voltage and power dissipation. The post-layout simulation results demonstrate that the proposed 3.4–10.1 GHz UWB LNA accomplishes a maximum gain of 14.26 dB with only 2.33 mW power consumption at 0.8 V supply voltage, while Noise Figure (NF) is 1.49–3.41 dB and the chip area is 0.46 mm^2 including test pads (core area is 0.23 mm^2).

Keywords: UWB; LNA; multiple-feedback network; low voltage; low power.

1. Introduction

Since the 3.1–10.6 GHz frequency band is released by the Federal Communications Commissions for civil use without licenses permission, the Ultra-wideband (UWB) radio has become more and more attractive both in academia and industry. As possessing merits of low cost, robustness and flexibility, it is extremely suitable for rapid speed and short distance wireless communication systems.[1,2] Furthermore, it is much convenient to fabricate the UWB receiver in a single chip with the development of advanced Complementary Metal Oxide Semiconductor (CMOS) technology. Compared with the blossom of UWB wireless communication system, the battery capacity improvement of battery-powered portable devices is relatively slow, so the

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circuit design for lower supply voltage and less power consumption without compromising other device performances is still a challenge.[3]

The Low-noise Amplifier (LNA) is a significant and the first active component in the UWB wireless receiver, which amplifies signals received by antenna to subsequent components and its performance will essentially influence the whole system.[4] Therefore, in the process of design, we should ensure that the UWB LNA supply enough power gain while import as lower noise as possible. Moreover, other characteristics of UWB LNA, such as good linearity and decreased die size occupation are also important to overall receiver chain.[5,6]

As the UWB spectrum ranges from 3.1 to 10.6 GHz, to utilize the spectral band as completely as possible, the UWB LNA should provide a wideband input impedance matching over a bandwidth about 7 GHz, it is much difficult and sophisticated than traditional single-frequency or narrow band LNA.[7] Many recently published papers have demonstrated their work on acquiring acceptable CMOS-based UWB LNA by utilizing diverse circuit structures, such as Common-gate (CG), resistive shunt feedback, distributed and L-degenerated (LG) LNA topology, while adopting techniques including current-reuse and transconductance g_m boosting.[8–11]

In this work, we propose a UWB LNA which utilizes a novel multiple-feedback input network constructed by shunt feedback resistor with transformer and configures all the cascaded transistors by current-reuse with forward body bias technique to achieve lower noise figure (NF), better gain and reverse isolation, while requiring moderate supply voltage and consuming minimal power dissipation. The paper is organized as follows: In Sec. 2, we firstly demonstrate the advantages and disadvantages of several topologies for bandwidth extension while exploring current-reuse and forward body bias techniques for low power operation, and then we illustrate the complete schematic of the improved UWB LNA. In Sec. 3, the proposed LNA is analyzed in different aspects including input/output matching, gain and NF. Post-layout simulation results and conclusions are discussed in Secs. 4 and 5, respectively.

2. Circuit Design Consideration

2.1. *Bandwidth extension*

The circuit schematics commonly used for bandwidth extension, such as CG LNA, resistive shunt feedback LNA, Distributed Amplifier (DA) LNA and LD LNA, are shown in Fig. 1.

By matching the input impedance to 50 Ω, the noise factor NF (NF(dB) = $10\log_{10}$NF) of CG LNA (shown in Fig. 1(a)) can be summarized as follow:

$$\mathrm{NF} = 1 + \frac{\gamma}{\alpha} + \frac{4R_s}{R_L} \tag{1}$$

where γ is a noise parameter, $\alpha = g_m/g_{d0}$ and g_{d0} is the channel conductance when $V_{\mathrm{DS}} = 0$ from channel thermal noise of $4\mathrm{k}T\gamma g_{d0}\Delta f$. In Eq. (1), setting a typical value

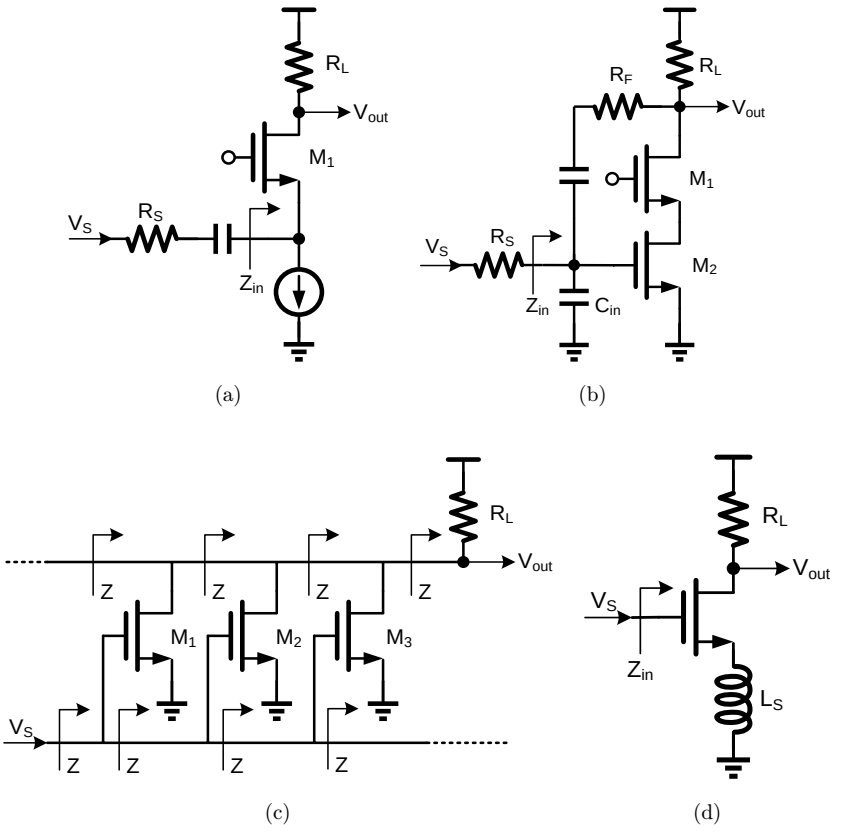

Fig. 1. Circuit schematics commonly used for bandwidth extension (a) Common-gate; (b) Resistive shunt feedback; (c) Distributed amplifier; and (d) L-degenerated.

for $\gamma/\alpha = 1.33$, to constrain the NF less than 5 dB, the R_L will be larger than 240 Ω. In 0.18 μm CMOS process, the bandwidth can hardly be extended and following circuit after LNA like down-conversion mixers cannot be driven as $R_L \geq 180\,\Omega$. Meanwhile, other noise sources will deteriorate the NF, so CG LNA is not a proper solution for UWB receiver.[12]

As displayed in Fig. 1(b), input impedance of the resistive shunt feedback LNA is derived as:

$$Z_{\text{in}} = C_{\text{in}}//[R_F + R_L/(1 + g_{m1}R_L)] \tag{2}$$

Assuming that given a 20 mW power consumption with 1.8 V voltage supply, then $I_D = 11.1$ mA. The maximum acceptable R_L will be 116 Ω, the feedback resistor R_F and gain A_V can be obtained from:

$$\begin{cases} R_F = 50(g_{m1}R_L + 1) - R_L = 193.84\,\omega \\ A_V = R_L(1 - g_{m1}R_F)/R_F + R_L = 9.2\,\text{dB} \end{cases} \tag{3}$$

and the noise factor can be calculated out by substituting parameters into subsequent equation:

$$\mathrm{NF} = 1 + \frac{R_F}{R_S}\left(\frac{1+g_{m1}R_S}{1-g_{m1}R_F}\right)^2 + \frac{1}{R_S R_L}\left(\frac{R_F+R_S}{1-g_{m1}R_F}\right)^2 + \frac{\gamma g_{m1}}{\alpha R_S}\left(\frac{R_F+R_S}{1-g_{m1}R_F}\right)^2$$
$$= 4.9\,\mathrm{dB}(\gamma/\alpha = 1.33) \tag{4}$$

To achieve better NF performance and higher frequency, this LNA will consume more power, which reduces its attractiveness for low power applications.[13]

Figures 1(c) and 1(d) reveal the topologies of DA LNA and LD LNA, respectively. Both of them can provide acceptable impedance matching, while the requirements of high-quality transmission line in DA LNA and high-Q inductors in LD LNA make them unsuitable for low-cost occasions because of large chip area occupation.[14,15]

Generally, the interstage parasitic capacitance limits bandwidth of the LNA which is often cascaded to the next stage. Taking circuit in Fig. 2(a) for an instance, the parasitic gate-source capacitor C_{GS} bypasses with load R_L, so it will reduce the bandwidth at frequency of $1/R_L C_{\mathrm{GS}}$. To alleviate this issue, a practical way is creating a series peaking in frequency response by a series inductance L across R_L and C_{GS} which resonates out the C_{GS}, like circuit architecture in Fig. 2(b).

As the series inductor produces a resistor-inductor-capacitor (RLC) resonant circuit with R_L and C_{GS}, the $|V_{\mathrm{out}}/I_{\mathrm{in}}|$ can be derived as follows:

$$\left|\frac{V_{\mathrm{out}}}{I_{\mathrm{in}}}\right| = \frac{\left(\frac{\frac{1}{sC}\cdot(sL+R)}{\frac{1}{sC}+sL+R}\right)}{\frac{sL+R}{R}} = \frac{R}{sLC+sRC+1} \tag{5}$$

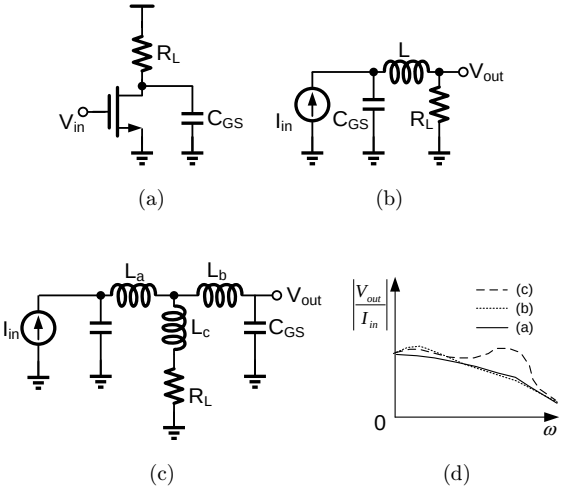

Fig. 2. Different LNA architectures and its frequency response (a) Common-source amplifier with parasitic capacitance; (b) Series inductive peaking; (c) Series-shunt-series peaking; and (d) Frequency response.

To further improve frequency response, a series-shunt-series circuit structure, which is constructed by triple inductors in Fig. 2(c), achieves better representation in frequency response (charted in Fig. 2(d)) than circuits of Figs. 2(a) and 2(b).[16]

2.2. *Low voltage operation*

As more and more components are inserted into LNA topology to acquire desirable performance, the consumption of power is exploded and the allowable bias current is constrained. Therefore, solutions to relieve these problems without degenerating LNA performance are desired. Conventionally, transistors are biased in weak inversion region, whose bulk is often grounded with source electrode or connected to low-level voltage. To some context, this technique reduces the power consumption because of lower current and lower overdrive voltage, but potential penalties including frequency restriction and unreliability are not ignorable. Meanwhile, transistors with low supply voltage in weak inversion will degrade NF and gain of LNA, so the forward body bias technique with current-reuse configuration is utilized to prevent the degradation issues.[17]

The relation between threshold voltage V_{th} and bulk-source voltage V_{bs} is expressed as:

$$V_{\text{th}} = V_{\text{tho}} + \gamma\left(\sqrt{2\phi_f - V_{\text{bs}}} - \sqrt{2\phi_f}\right) \tag{6}$$

where V_{th0} is the threshold voltage when $V_{\text{bs}} = 0$, and the bulk-effect coefficient γ with the bulk Fermi potential ϕ_f. From Eq. (6), it is obvious that the threshold voltage can be operated by the bulk-source voltage, the former one is decreasing with the increasing latter one. However, the threshold voltage cannot be diminished immoderately, as the forward-bias positive-negative (PN) junction leakage current originated from the parasitic substrate-source diode will not be negligible as soon as the bulk-source voltage exceeds a specific value. Figure 3 exposes the correlations of threshold voltage and leakage current versus bulk-source voltage.

From Fig. 3, it is clear that the body leakage current grows rapidly when the bulk-source voltage surpasses 0.5 V, which implies that the body leakage current cannot be neglected if the bulk-source voltage exceeds the PN junction turn-on voltage. Therefore, in this LNA design, the bulk-source voltage V_{bs} of each transistor is biased at 0.44 V and V_{th} decreases from 0.51 to 0.42 V, then the V_{gs} of each transistor could be relatively lower. Nevertheless, as discussed in last two paragraphs, low V_{gs} will make transistors enter into weak inversion region, which will introduce large NF and constrain bandwidth extension. This is not desirable for an UWB LNA, so the supply voltage V_{DD} is set at 0.8 V and the gate of transistor M_1 is biased with V_{G1} at 0.57 V, this configuration ensures that the overdrive voltage $(V_{\text{gs}} - V_{\text{th}})$ will not be too small and all two transistors (M_1 and M_2) will be in the strong inversion operation.

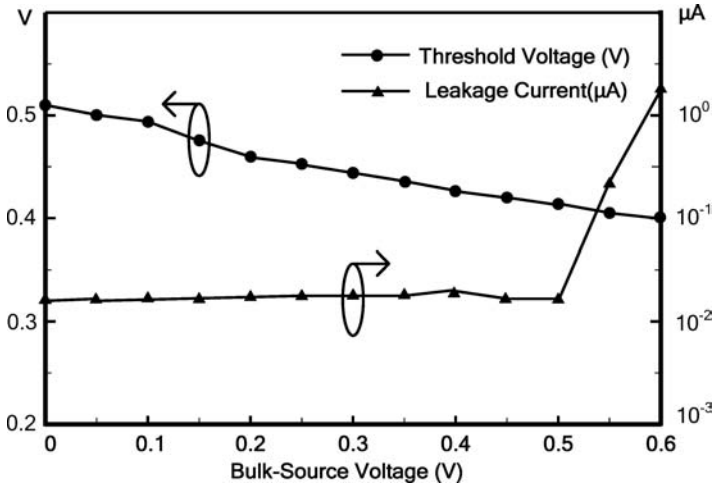

Fig. 3. Correlations of threshold voltage and leakage current versus bulk-source voltage.

As above-mentioned, the supply voltage of the LNA could be reduced by applying forward body biasing technique. Not only that, other performances in terms of gain, NF, input/output impedance matching and power dissipation can also be adjusted by forward body basing configuration. According to Eq. (6), the drain current can be influenced by the bulk-source voltage $V_{\rm bs}$ as well as $V_{\rm th}$, then the bulk transconductance $g_{\rm mb}$ can be expressed as:

$$g_{\rm mb} = \frac{\partial I_D}{\partial V_{\rm bs}} = g_m \frac{\gamma}{2\sqrt{2\varphi_f + V_{\rm sb}}} = \eta g_m. \tag{7}$$

Therefore, the gain of the cascode topology amplifier configured by forward body biasing technique can be calculated as:

$$A_v = \frac{V_{\rm out}}{V_{\rm in}} = (g_{m1} + g_{mb1}) r_{O1} [(g_{m2} + g_{mb2}) r_{O2} + 1] \tag{8}$$

The above equation indicates that the gain will be improved by the bulk transconductance increasement of M_1 and M_2. Meanwhile, the induced gate noise, which is inversely proportional to the transconductance of transistor, will be enlarged if the $V_{\rm gs}$ is reduced, especially when the transistors enter into the weak inversion region, while the NF will be greatly increased due to the enlargement of the induced gate noise. The total transconductance of a transistor with forward body biasing will be increased from g_m to $[(1+\eta)g_m]$ (illustrated in Eq. (7)), then the induced gate noise can be restrained to lower. That is to say, both the gain and NF performance would be enhanced with a lower supply voltage through the forward body biasing. Furthermore, the input and output impedance of the cascode LNA are separately related to the gate-source capacitance $C_{\rm gs}$ of the transistor M_1 and M_2 (In Sec. 3, this issue

will be analyzed in detail). And capacitance C_{gs} depends on threshold voltage V_{th} of transistors, thereby relating to bulk-source voltage V_{bs}. In other words, the input/output impedance could be modified by the bulk-source voltage, which means the forward body biasing technique gives a degree of freedom to the input/output matching adjustment.

2.3. *Proposed LNA*

Based on the bandwidth extension analysis and low voltage operation consideration of Secs. 2.1 and 2.2, the cascode topology LNA with multi-feedback is displayed in Fig. 4. The common-source stage of this LNA adopts multiple-feedback network to accomplish bandwidth extension, while the CG stage is buffered and gain-improved with inductive peaking configuration.

For low-voltage and low-power operation, all transistors are adjusted by forward body bias technique without compromising demanded device characteristic, and transistor M_1 in the common-source stage reuses the bleeding current of the CG stage transistor M_2 to further decrease power consumption of the entire LNA. As a result of a series-shunt-series circuit with triple inductors is equal to double

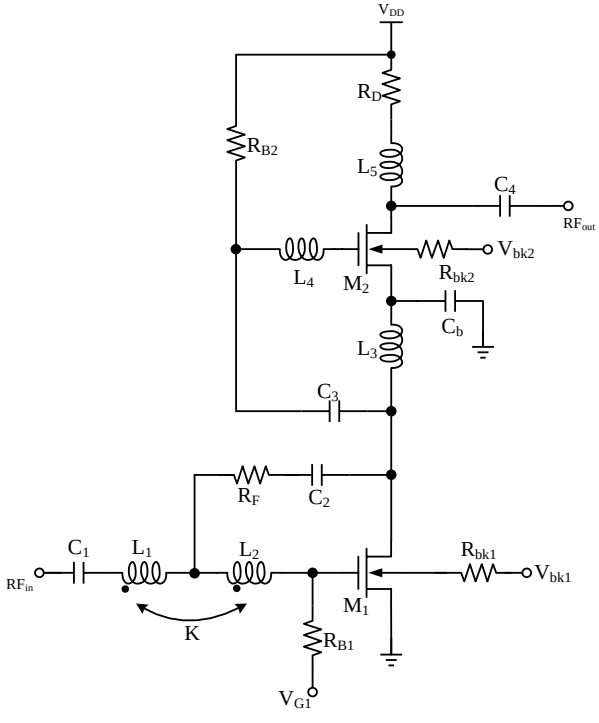

Fig. 4. The topology of the proposed LNA.

mutual-inductance inductors, inductor L_1 and L_2 constitute as primary and secondary coil of a transformer to save chip area, while K is the magnetic coupling coefficient between L_1 and L_2. Resistor R_F across gate and drain of M_1 sends back the AC small signal and produces a resistive shunt feedback second-order band-pass filter which constructs the multiple-feedback network with transformer. Interstage matching is completed by L_3 and L_4. L_5 is inserted between M_2 and R_D as part of the load to improve gain flatness and to eliminate the parasitic capacitance of M_2 drain.

3. Circuit Analysis

3.1. *Input matching*

For maximum power transfer, impedance matching is crucial for LNA, especially over such a wide bandwidth in UWB receiver. Traditionally, a certain number of inductors are adopted to construct LC network while occupy too much chip area and the parasitic effects are not ignorable, hence the input stage is configured by transformer and shunt feedback resistor based on common-source amplifier which has better quality factor and higher gain. The small signal equivalent circuit of the input matching stage network is shown in Fig. 5.

Where V_S is the input signal source and its impedance is R_S, while Z_{in} and Z_L are the input impedance of the LNA and the output impedance of transistor M_1, respectively. The transformer can be substituted by triple inductors for more convenient analysis and M is the coefficient of mutual inductance. Thus, the impedance of LNA Z_{in} can be derived as follow:

$$Z_{\text{in}} = S(L_1 + M) + \left[S(L_2 + M) + \frac{1}{SC_{\text{gs1}}}\right] // Z_F // S(-M) \tag{9}$$

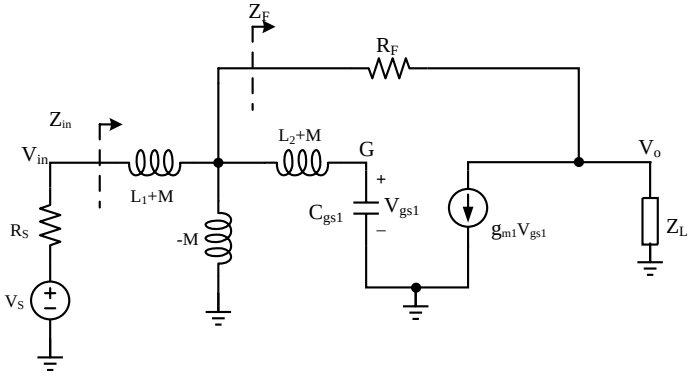

Fig. 5. The input network of proposed LNA.

where

$$Z_F = \frac{R_F + Z_L}{1 + \dfrac{g_{m1}}{S^2 C_{\mathrm{gs1}}(L_2 + M) + 1} \cdot Z_L}. \tag{10}$$

There are multiple-frequency poles in Eq. (9). The Z_F plays an important role in low-frequency poles. Ignoring the inductance loss and assuming that

$$\begin{cases} S^2 C_{\mathrm{gs1}}(L_2 + M) \gg 1 \\ g_{m1} Z_L \gg 1 \end{cases} \tag{11}$$

then we get

$$Z_F = \frac{1}{g_{m1}} + \frac{R_F}{g_{m1} Z_L}. \tag{12}$$

High-frequency poles are manly influenced by L_2, M and C_{gs}. To get an ideal trade-off between bandwidth and other performances, device parameters of input matching network have been adopted as: $L_1 = 0.18\,\mathrm{nH}$, $L_2 = 1.42\,\mathrm{nH}$, $R_F = 708\,\Omega$, $K = 0.69$, $W_1 = 92\,\mu\mathrm{m}$.

3.2. *Output matching*

Generally, the component after LNA is the filter or mixer, output stage matching of LNA is important to signal transmission. It is common that output matching is realized by active device like source-follower which decreases linearity and gain. Meanwhile, passive devices also have been used but occupy too much chip area. This proposed LNA utilizes CG structure with inductance peaking for output matching, of which output stage small signal equivalent circuit is displayed in Fig. 6.

From Fig. 6, the output impedance of LNA can be written as:

$$\begin{cases} Z_o = \dfrac{1}{\dfrac{1 + Z_g(\omega) g_{m2}}{Z_g(\omega) + \frac{1}{j\omega C_{\mathrm{gd2}}}} + \dfrac{1}{Z_2(\omega)}} \\ Z_g(\omega) = Z_{o1} // \dfrac{1}{j\omega C_{\mathrm{gs2}}} \end{cases} \tag{13}$$

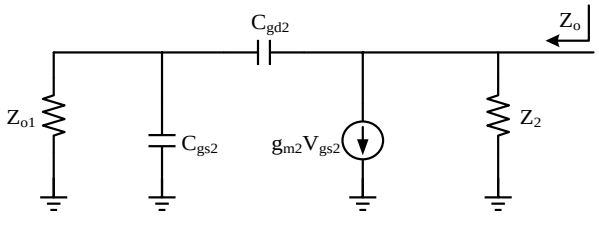

Fig. 6. The output network of proposed LNA.

At low frequencies, the parasitic capacitance C_{gs2} is negligible and $Z_o \approx R_d$, the output matching will be acceptable as setting $R_d = 50\,\Omega$. With frequency increases, C_{gs2} cannot be ignored, so L_5 is inserted to counteract this parasitic capacitance and get a better output matching without degrading the gain.

3.3. *Noise analysis*

As being the first active component of UWB receiver, the noise of LNA is significant to the whole RF front end. Furthermore, the common-source stage of LNA contributes major affect to the LNA NF. The main noise sources consist of feedback resistor, voltage/current bias circuit, input matching network and transistor channel noise.

Figure 7 shows the noise model of the input network, $\overline{e_{ns}^2}$ and $\overline{e_{nR_{EQ}}^2}$ are the noise sources of power supply and equivalent resistor. $\overline{i_{nout}^2}$ is the overall noise with the induced gate noise $\overline{i_{ng}^2}$ and the channel thermal noise $\overline{i_{nd}^2}$ of M_1. The operating frequency of the input network can be expressed as:

$$\omega_0 = \frac{1}{\sqrt{C_{gs1}[(L_1 + M) + ((-M)//(L_2 + M))]}}. \tag{14}$$

As resistor

$$R_P = (R_F/(1 - A_v))(1 + Q_{L_Z}^2) \tag{15}$$

is the parallel equivalent resistance of L_3, we can get the quality factor of the input network from Eq. (14):

$$Q_T = \frac{C_{gs1}/\omega_0}{R_s + \dfrac{\omega_0 (L(k+1))^2}{R_P}}. \tag{16}$$

According to Eqs. (14) and (16), the NF can be derived as:

$$\mathrm{NF} = \frac{R}{R_S}\left(1 + \frac{R}{R_S}\frac{\omega_0^2 R_S g_{m1}\gamma}{\omega_{T_0}^2 \alpha}\chi\right), \tag{17}$$

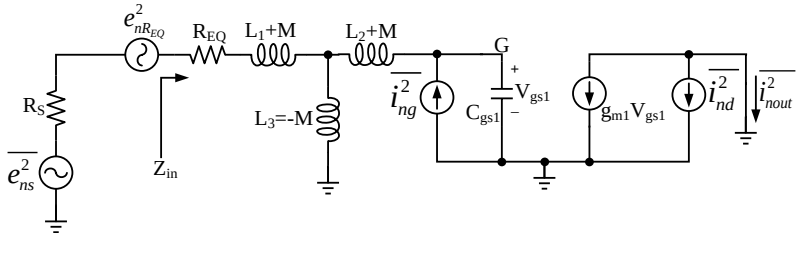

Fig. 7. Noise model of the input network.

where

$$\begin{cases} \chi = \dfrac{\delta\alpha^2}{5\gamma}[1+Q_T^2] + 1 - 2|c|\sqrt{\dfrac{\delta\alpha^2}{5\gamma}} \\ R = R_s + \dfrac{((L_1+M)\omega_0)^2}{R_F/(1-A_v)} \end{cases} \tag{18}$$

and induced gate noise factor is δ. c is the coefficient of induced gate noise and channel thermal noise. To decrease the noise of LNA, we can reduce the transconductance of M_1, but the gain will be degraded. Meanwhile, the increasement of feedback resistor R_F can also enhance the noise performance but the bandwidth will be limited. All these parameters should be cautiously considered to get an agreeable balance between gain and noise performance.

3.4. *Gain analysis*

Because the proposed LNA is a cascode topology LNA, the gain of it should be calculated in two steps. The small signal equivalent circuit of the entire LNA is displayed in Fig. 8.

In the common-source stage, the gain will be:

$$A_1 = \frac{V_{o1}}{V_{\text{in}}} = \frac{1}{S(L_1+M)\left(\dfrac{\frac{1}{S(L_1+M)} + \frac{1}{R_F} + g'_{m1}}{(R_F//Z_L)\left(\frac{1}{R_F - g'_{m1}}\right)} - \dfrac{1}{R_F}\right)} \tag{19}$$

where

$$g'_{m1} = \frac{g_{m1}}{SC_{\text{gs1}}[((L_2+M) + \dfrac{1}{SC_{\text{gs1}}})//(-SM)]} \tag{20}$$

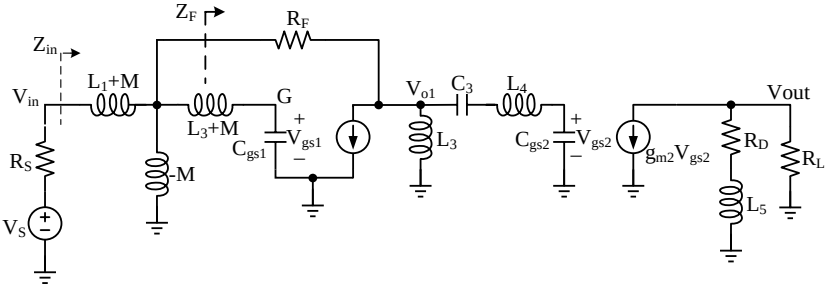

Fig. 8. Noise model of the proposed LNA.

The gain of the CG stage can be expressed as:

$$A_2 = \frac{V_{\text{out}}}{V_{o1}} = \frac{-g_{m2}[R_L//(R_L + SL_5)]}{S^2 L_4 C_{\text{gs2}} + (1 + \frac{C_{\text{gs2}}}{C_3})} \tag{21}$$

$$\approx -g_{m2} \cdot (R_D + SL_5) \tag{22}$$

From Eq. (19) we get that the gain increases by enlarging the feedback resistor. And Eq. (22) indicates that the gain also can be enhanced by increasing g_{m2} or R_D while power consumption and output matching will not be desirable. To get a proper compromise among these performances, we set parameters as follow: $C_1 = 5\,\text{pF}$, $L_1 = 0.18\,\text{nH}$, $L_2 = 1.42\,\text{nH}$, $W_1 = 92\,\mu\text{m}$, $R_F = 708\,\Omega$, $C_2 = 7.08\,\text{pF}$, $L_3 = 11.47\,\text{nH}$, $C_3 = 0.65\,\text{pF}$, $L_4 = 1.09\,\text{nH}$, $C_b = 10\,\text{pF}$, $W_2 = 111\,\mu\text{m}$, $C_4 = 13.3\,\text{pF}$, $R_D = 69\,\Omega$, $L_5 = 1.44\,\text{nH}$.

4. Results and Discussions

The proposed UWB LNA is implemented by Cadence IC Design Tools Spectre RF simulator under standard Charted $0.18\,\mu\text{m}$ RF CMOS technology. As we adopted forward body bias and current-reuse techniques for low power operation, to get a lower supply voltage with a moderate leakage current, we set body bias voltage $V_{\text{bk1}} = V_{\text{bk2}} = 0.44\,\text{V}$ and add the current restrict resistors $R_{\text{bk1}} = R_{\text{bk2}} = 8\,\text{k}\Omega$ to the body terminals of all transistors, then the supply voltage V_{DD} reduces to 0.8 V. Other parameters for realizing these techniques are: $V_{\text{G1}} = 0.57\,\text{V}$, $R_{\text{B1}} = R_{\text{B2}} = 8\,\text{k}\Omega$.

The scattering parameter simulation results of the proposed UWB LNA are displayed from Figs. 9–12 (S11, S22, S12, S21). Figure 9 is the input return loss (S11)

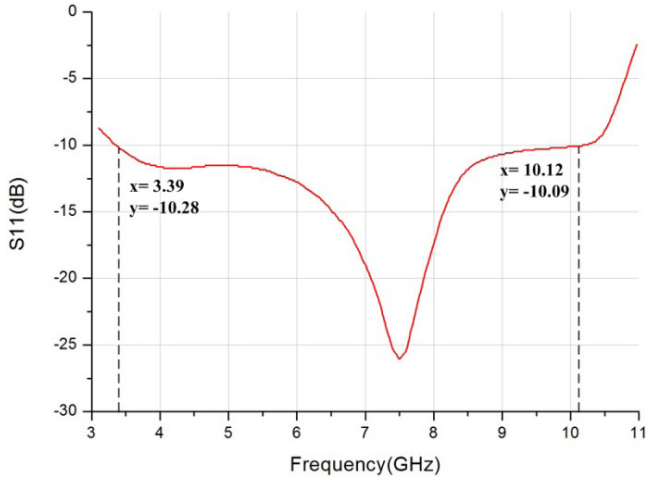

Fig. 9. Input return loss (S11) versus frequency.

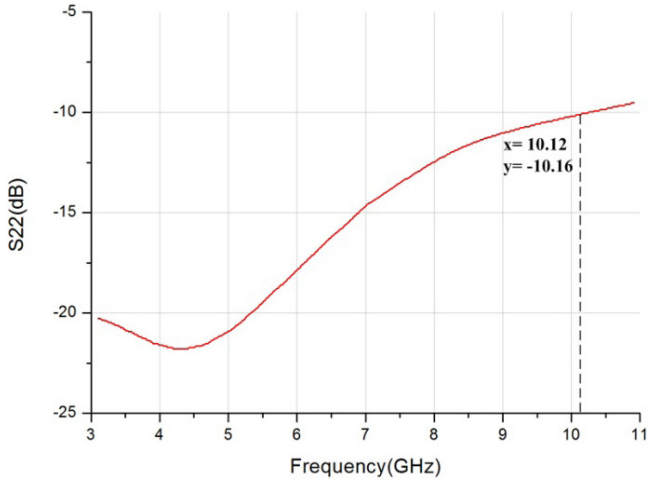

Fig. 10. Output return loss (S22) versus frequency.

of the LNA versus frequency. Parameter S11 indicates the performance of input matching and it is obvious to figure out that the S11 is less than −10 dB from 3.4 to 10.1 GHz. Meanwhile, in Fig. 10, the output return loss (S22) is also less than −10 dB versus frequency over 3.4–10.1 GHz. As both S11 and S22 are less than −10 dB, the proposed UWB LNA can provide good input and output matching over the desired frequency.

The reverse isolation (S12) is shown in Fig. 11 and it is below −30 dB, so the signal of output terminal is well isolated from the input terminal in this UWB LNA. From 3.4 to 10.1 GHz, the power gain (S21) of the proposed UWB LNA is

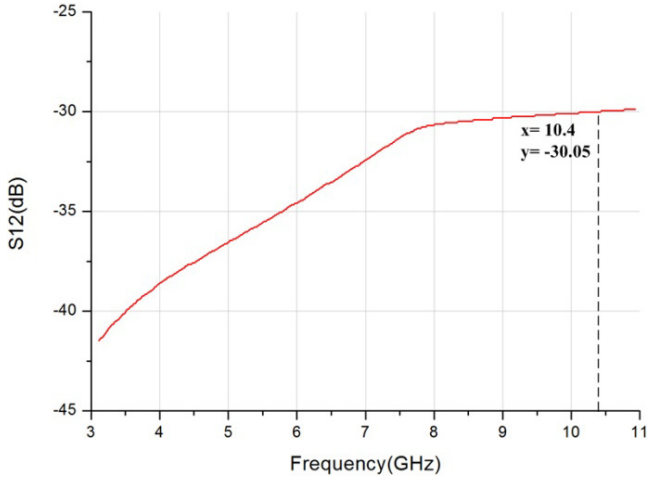

Fig. 11. Reverse isolation (S12) versus frequency.

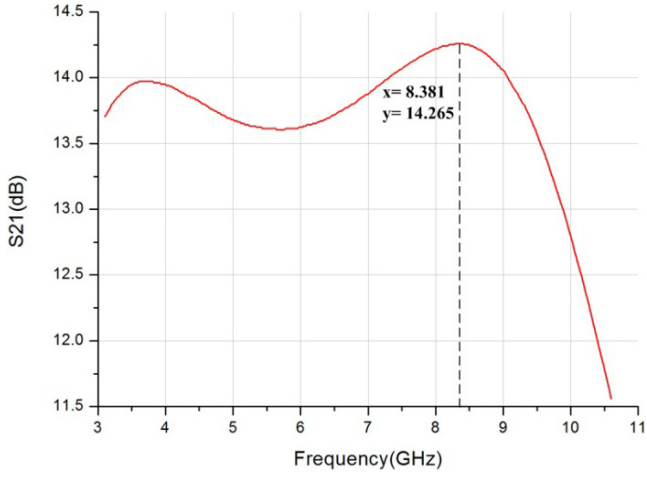

Fig. 12. Power gain (S21) versus frequency.

larger than 12 dB and acquires a maximum value of 14.26 dB at 8.4 GHz (charted in Fig. 12). Furthermore, the 3-dB bandwidth also covers the frequency over 3.4–10.1 GHz.

Although this LNA achieves acceptable performance in scattering parameters, it does not compromise the NF. Figure 13 shows that the NF of the proposed UWB LNA ranges from 1.49 to 3.41 dB over the band of interest and has a minimal NF of 1.49 dB at 8.28 GHz. Usually, the IIP3 is an important index of the linearity performance, but the UWB LNA rarely suffers from the gain compression issue because

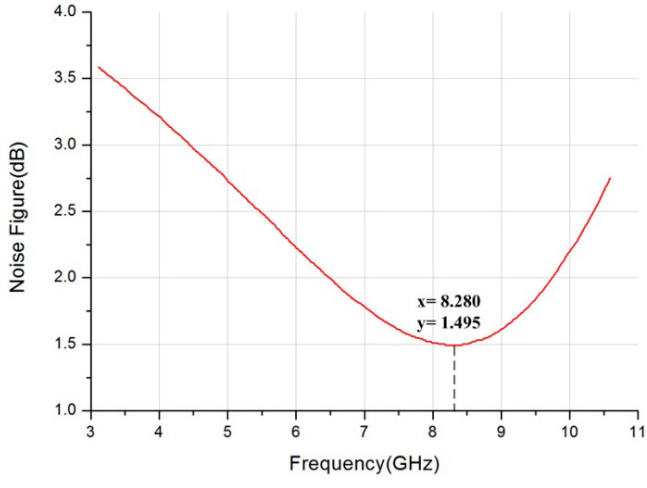

Fig. 13. NF versus frequency.

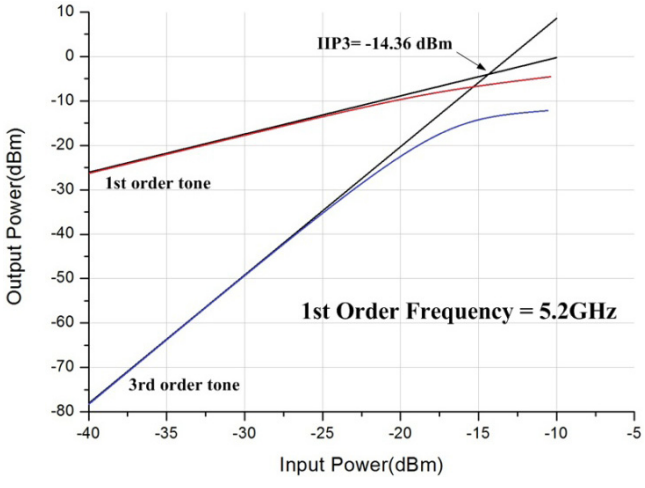

Fig. 14. IIP3 of the proposed UWB LNA at 5.2 GHz.

the input signal power is often not very large. At the 5.2-GHz frequency, simulation result of the IIP3 is −14.36 dBm (Fig. 14). The IIP3 can be increased by some techniques while it will consume more power and reduce the gain. In battery-powered portable devices, lower power consumption with relatively reduced linearity performance can also be acceptable.

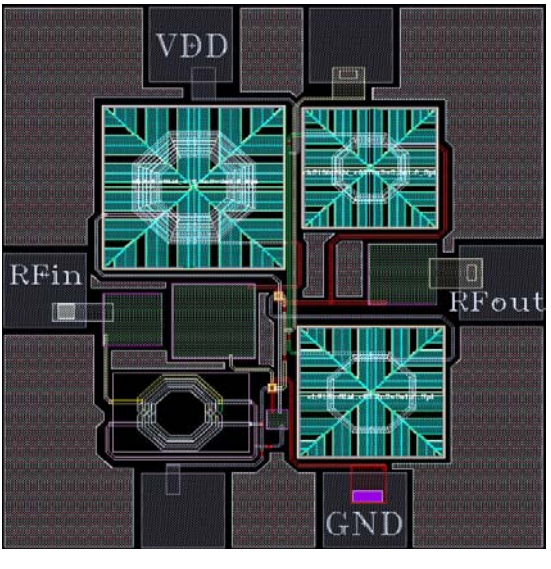

Fig. 15. The layout diagram of the proposed UWB LNA.

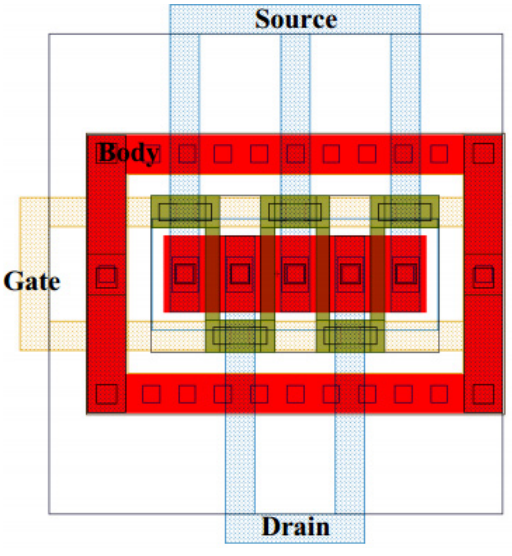

Fig. 16. The enlarged layout view of the transistor.

The layout diagram of the proposed LNA is presented in Fig. 15, which occupies a compact chip area of about $0.64 \times 0.72\,\text{mm}^2$ including the testing pads (core area is $0.41 \times 0.49\,\text{mm}^2$) because of adopting a transformer instead of triple inductors in the input matching network. An enlarged layout view of the transistor is drawn in Fig. 16 to demonstrate the realization of the forward body biasing technique under the standard Charted $0.18\,\mu$m RF CMOS technology. The transistor in Fig. 16 has four fingers, the gate-poly is connected through metal layer 1, the source and drain terminals are connected using metal layer 2. The body of the transistor is formed by using a guard ring, the basing supply voltage is connected to the guard ring for realizing the forward body biasing technique and giving a shield to the transistor cell.

To further test the performance of this proposed UWB LNA under different conditions, whose S11, S21 and NF for three corners including typical process (65°, corner 1), fast process (−25°, corner 2) and slow process (100°, corner 3) are simulated in Fig. 17. The first three figures in Fig. 16 demonstrate the performance of S11, S21 and NF for three corners, while corner 2 possesses better performances than other two corners. S11, S21 and NF versus temperature for three corners at 7 GHz are charted in last three figures of Fig. 17, and all performances in three corners degrade at high temperature.

The comparison of the proposed UWB LNA with other reported works is listed in Table 1, and the UWB LNA without the forward body biasing technique is also simulated to further reveal the benefit of this technique. From this table, it is clear that the proposed UWB LNA possesses merits of high gain, reduced NF at lower

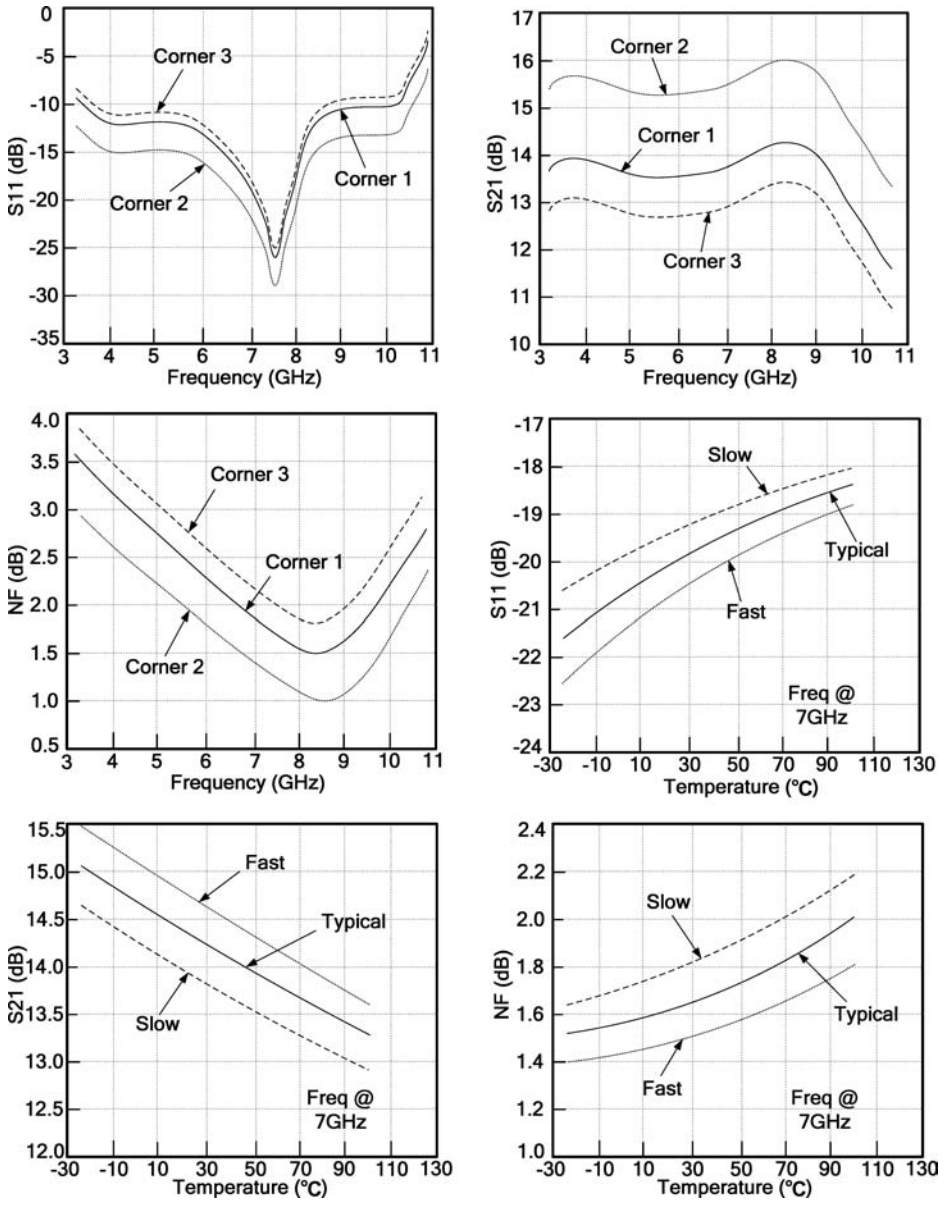

Fig. 17. Simulation results of the proposed UWB LNA for three corners.

supply voltage with minimal power consumption and smaller chip area than most of the other previously reported works, and the forward body biasing technique really makes this proposed UWB LNA has better performances in many aspects, especially in low supply voltage and low power dissipation.

Table 1. Performances comparison of UWB LNA.

References	1		2		5		7		This work (SIM)	
MEA/SIM[a]	MEA	SIM	MEA	SIM	MEA	SIM	MEA	SIM	noFBB[b]	FBB[c]
Supply (V)	1.2	—	1	—	1.2	—	1.5	—	**1.2**	**0.8**
Power (mW)	16.0	—	7	—	7.2	—	13.4	—	**6.8**	**2.33**
NF_{min} (dB)	3.1	2.2	4.5	4.0	3.0	2.7	2.5	2.2	**2.6**	**1.49**
$Gain_{max}$ (dB)	16.0	16.8	14.5	15.1	12.5	14.1	12.7	13.6	**13.7**	**14.2**
S11 (dB)	<-10.5	—	<-10	<-11	<-9	<-9	<-9	<-11	$<$ **− 10**	$<$ **− 10**
S22 (dB)	<-10	—	<-13	<-15	—	—	—	—	$<$ **− 10**	$<$ **− 10**
S12 (dB)	—	—	—	—	<-45	<-45	<-45	—	$<$ **− 30**	$<$ **− 30**
IIP3 (dBm)	−5.4	—	−4.8	—	—	—	−3	—	**− 15.6**	**− 14.3**
Bandwidth	3.0–8.5	—	3.1–10.6	—	2.6–10.2	—	3.1–10.3	—	**3.4–10.1**	**3.4–10.1**
Technology	0.09	—	0.13	—	0.09	—	0.18	—	**0.18**	**0.18**
Area (mm^2)	0.022	—	1	—	0.64	—	0.68	—	**0.23**	**0.23**

[a]MEA = measured results, SIM = simulated results.
[b]noFBB = LNA without forward body biasing technique.
[c]FBB = LNA with forward body biasing technique.

5. Conclusion

In this paper, a 3.4–10.1 GHz high gain low voltage low power CMOS LNA for UWB receiver is presented, which utilizes a multiple-feedback network constructed by shunt feedback resistor with transformer to realize desirable bandwidth extension and reduce chip area occupation in the input stage. All the cascaded transistors are configured by current-reuse structure and adjusted by forward body bias technique to further reduce supply voltage and minimize power consumption. By using techniques and making improvements in circuit design of this LNA, it can achieve a maximum power gain of 14.2 dB at 0.8 V supply voltage with only 2.33 mW power consumption while the NF is well constrained under 3.41 dB with a minimum value of 1.49 dB. All these characteristics make this LNA to be adopted in the implementation of many UWB applications, especially in some applications that require low supply voltage and reduced power consumption.

Acknowledgments

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