A universal emulator for memristor, memcapacitor, and meminductor and its chaotic circuit

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ABSTRACT

In this paper, a universal charge-controlled mem-elements (including memristor, memcapacitor, and meminductor) emulator consisting of off-the-shelf devices is proposed. With the unchanged topology of the circuit, the emulator can realize memristor, memcapacitor, and meminductor, respectively. The proposed emulation circuit has a simple mathematical relationship and is constructed with few active devices and passive components, which not only reduces the cost but also facilitates reproduction and facilitates future application research. The grounding and floating forms of the circuit are demonstrated, and Multisim circuit simulation and breadboard experiments validate the emulator's effectiveness. Furthermore, a universal mem-elements chaotic circuit is designed by using the proposed mem-elements emulator and other circuit elements, which is a deformation circuit of Chua's dual circuit. In this circuit, no matter whether the mem-element is memristor, memcapacitor, or meminductor, the chaotic circuit structure does not change, and all can generate hyper-chaos.

The memristor is the fourth fundamental circuit element. Based on the conception of memristor, memcapacitor and meminductor are proposed as two newly generalized energy storage components. In order to facilitate the follow-up study, the emulators of these three components are successively proposed by the researchers. However, in previous literatures, all the emulator circuits can only emulate the behavior of one of the mem-elements, and there is no unified mem-elements circuit structure which can mimic three mem-elements. In this paper, a universal charge-controlled mem-elements emulator consisting of off-the-shelf devices is proposed. With the unchanged topology of the circuit, the emulator can realize memristor, memcapacitor, and meminductor by replacing a resistor or a capacitor. In addition, because of the unique electrical properties of memristor, memcapacitor, and meminductor, they are usually employed to construct chaotic circuits. In this paper, we design a novel chaotic circuit based on our proposed mem-elements emulator, which is characterized by connecting different mem-elements at the same position and then hyper-chaos can be observed by setting the circuit parameters.

I. INTRODUCTION

In 1971, by studying the relationship between current i, voltage v, charge q, and flux φ, Chua[1] concluded that in addition to resistor, capacitor, and inductor, there should be a new basic two-terminal circuit element, which is called as a memristor to represent the mathematical relationship between charge q and flux φ. In 2008, Strukov and his group in HP lab first fabricated a physical memristor, which is a two-terminal nanoscale electronic device based on TiO_2 material.[2] Thus, memristor's place was cemented as the fourth fundamental circuit element.

Based on the conception of memristor, memcapacitor and meminductor are proposed as two newly generalized energy

storage components.[3] Memristor, memcapacitor, and meminductor are collectively referred to as mem-elements.[42] The unique memory characteristics and nanoscale structures of these three mem-elements have a wide application prospect in non-volatile memory,[4] artificial neural networks,[5–10] and chaotic circuits.[11–15]

However, due to the cost and technical difficulties of nanoscale device manufacturing, commercially available mem-elements will be impossible in the near future. Therefore, in order to explore the follow-up application of these three mem-elements, the studies of their simulation models and emulator circuits are very necessary. Indeed, some research groups have proposed many emulator circuits for memristor. Kim *et al.*[16] designed a memristor emulator with off-the-shelf solid state devices and further improved it in another literature[17] to make its experimental results similar to the real HP TiO_2 memristor. However, the emulator contains CMOS and a variety of active devices and passive components, so the circuit structure is complex and bulky. In Refs. 11–18, memristor emulators were all designed based on operational amplifiers. However, the circuit based on operational amplifiers has disadvantages such as low linearity, large supply voltage, small voltage fluctuation, and limited operating frequency. These disadvantages are overcome in some studies which use second-generation current conveyor (CCII).[19–22] In Ref. 22, a floating analog memristor emulator based on CCII was proposed, which uses fewer active and passive devices. However, it is a flux-controlled model different from the real HP memristor which is charge-controlled. Recently, high frequency incremental/decremental memristor emulators were built using single current mode module,[23,24] but they cannot be implemented in hardware because there are no existing components to implement those modules. With the extensive research of memristor emulators, the research involved the emulators of memcapacitor and meminductor has gradually attracted the interest of researchers. Some converters for emulating memcapacitor and meminductor were proposed in Refs. 25–28 based on the memristor emulator and active devices. Among them, Yu *et al.* proposed a universal converter for transformations among memristor, memcapacitor, and meminductor by making use of active devices, a memristor, some resistors and capacitors.[28] However, it[28] needs to change the properties of the elements in five positions to carry out the conversion among three mem-elements, so it is very complicated. In Refs. 29 and 30, Fouda and Radwan proposed the memristor-less memcapacitor and meminductor emulators, respectively, but only in the grounded form. Sah *et al.* implemented a meminductor circuit emulator,[31] but the circuit is bulky because of containing multiple CMOS current mirrors. In Ref. 32, a flux-controlled meminductor emulator consisting of two operational amplifiers, four CCIIs, and a multiplier was proposed.

In above literatures, all the emulator circuits can only emulate the behavior of one of the mem-elements, and there is no unified mem-elements circuit structure which can mimic three mem-elements in same circuit topology. In this paper, a new universal charge-controlled mem-elements emulator consisting of off-the-shelf devices is proposed. The emulator is made up of three CCII+s, a multiplier, and several resistors and capacitors, which makes hardware implementation easy. And in the case that the overall circuit topology remains unchanged, the proposed emulator can achieve the emulation of three mem-elements by replacing one resistor or capacitor in the circuit.

The application of mem-elements to chaotic circuits is an important research topic. Some different memristor emulators have been proposed and applied to different chaotic circuits to generate various chaotic phenomena,[11–15,33–39] Indeed, simulation analyses show that not only memristor but also memcapacitor and meminductor can be used to construct chaotic oscillator. Recently, many researchers proposed some new memcapacitor and meminductor models and designed chaotic oscillators based on the proposed models. In Ref. 40, a memcapacitor chaotic oscillator with two unstable equilibriums was reported. Yuan *et al.* proposed new memcapacitor and meminductor models and use them to construct generators for generating chaos, respectively, in Refs. 41 and 42. However, no literature has shown that three mem-elements emulators generate chaos by the same circuit topology. In this paper, a new chaotic oscillator based on our proposed universal emulator is designed, the MATLAB simulation analyses show when three mem-elements are respectively connected to the oscillator at the same position, hyper-chaos are all generated by adjusting the circuit parameters.

This paper is organized as follows. In Sec. II, the mathematical model of charge-controlled mem-elements is described. Grounding and floating universal charge-controlled mem-elements emulators are proposed in Sec. III. The experiment results and analyses are shown in Sec. IV. In Sec. V, the universal mem-elements chaotic circuit is designed and the numerical simulation is presented. Finally, this paper is concluded in Sec. VI.

II. MATHEMATICAL MODEL OF CHARGE-CONTROLLED MEM-ELEMENTS

In 2008, HP Labs successfully developed a nano-scale memristor based on metal and metal oxides.[2] It is composed of the undoped part and the doped part. The developed device and its equivalent circuit are shown in Fig. 1, where the memristance, M(t), is expressed as in the following equation:

$$\begin{aligned} M(t) &= R_{ON}\frac{w(t)}{D} + R_{OFF}\left(1-\frac{w(t)}{D}\right) \\ &= R_{OFF} + k(R_{ON}-R_{OFF})q(t) \\ &\approx R_{OFF} - kR_{OFF}q(t). \end{aligned} \tag{1}$$

Here, $q(t)$ is the integral of current $i(t)$ passing through the memristor, R_{OFF} and R_{ON} are the resistances of the undoped part and the doped part respectively, $w(t)$ is the state variable of the memristor that is limited by (0,D), D is the total length of the TiO_2 layer, and $k = \mu_v R_{ON}/D$ and μ_v is the mobility factor.

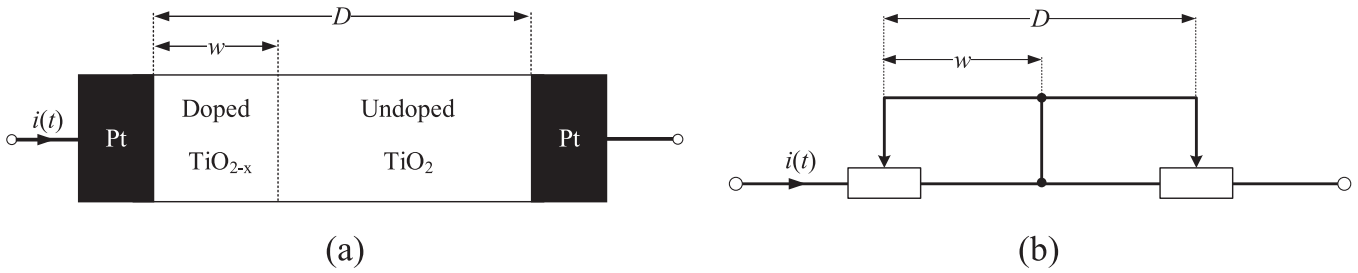


FIG. 1. HP memristor device and its equivalent circuit.

By Ohm's law, we have

$$\begin{aligned} v(t) &= M(t)i(t) \\ &= (R_{OFF} - kR_{OFF}q(t))i(t) \\ &= (a - bq(t))i(t) = M(q)i(t), \end{aligned} \tag{2}$$

where $a = R_{OFF}$ and $b = kR_{OFF}$.

In 2009, Di Ventra *et al.* extended the notion of memory elements from memristor to memcapacitor and meminductor, where the memcapacitor and meminductor are respectively defined as[3]

$$\begin{aligned} v_C(t) &= C_M^{-1}(x, q, t)q(t), \\ \dot{x} &= f(x, q, t), \end{aligned} \tag{3}$$

$$\begin{aligned} \varphi_L(t) &= L_M(x, i, t)i(t), \\ \dot{x} &= f(x, i, t), \end{aligned} \tag{4}$$

where $q(t)$ is the total charge on the memcapacitor at time t, $v_C(t)$ is the corresponding voltage, and $C_M^{-1}(x, q, t)$ is an inverse memcapacitance.[3] Similarly, $\varphi_L(t)$ is the accumulated flux on the meminductor at time t, $i(t)$ is the corresponding current, and $L_M(x, q, t)$ is a meminductance.

The above formulas of memcapacitor and meminductor can be converted to[3]

$$v_C(t) = C_M^{-1}[\int_{t_0}^{t} q(\tau)d\tau]q(t) = C_M^{-1}(\sigma)q(t), \tag{5}$$

$$\varphi_L(t) = L_M[\int_{t_0}^{t} i(\tau)d\tau]i(t) = L_M(q)i(t) \tag{6}$$

called as charge-controlled memcapacitor and charge-controlled meminductor, respectively. Here, σ is the integral of q with respect to time t.

The above three mem-elements have similar mathematical relations. Similar to formula (2) where $M(q) = a - bq(t)$, we can make $C_M{}^{-1}(\sigma) = a - b\sigma(t)$ and $L_M(q) = a - bq(t)$.[30] So, (2), (5), and (6) can be further expressed as follows:

Memristor:

$$v(t) = M(q)i(t) = [a - bq(t)]i(t) = a \cdot i(t) - b \cdot q(t)i(t), \tag{7}$$

Memcapacitor:

$$v_C(t) = C_M^{-1}(\sigma)q(t) = [a - b\sigma(t)]q(t) = a \cdot q(t) - b \cdot \sigma(t)q(t), \tag{8}$$

Meminductor:

$$\varphi_L(t) = L_M(q)i(t) = [a - bq(t)]i(t) = a \cdot i(t) - b \cdot q(t)i(t). \tag{9}$$

In above three formulas, a and b are real parameters. When b is negative, (7), (8), and (9) denote incremental models, and when b is positive, (7), (8), and (9) denote decremental models.

III. UNIVERSAL CHARGE-CONTROLLED MEM-ELEMENTS EMULATOR

The proposed universal charge-controlled mem-elements emulator circuit is shown in Fig. 2(a), which consists of three second generation current conveyors (CCII+s), one analog multiplier (AM), and five basic discrete components, where Y1 and Y2 (the yellow blocks) are resistors or capacitors. When they are both resistors, the emulator is equivalent to a memristor emulator. The emulator will be equivalent to a memcapacitor emulator just changing Y1 from resistor to capacitor, and a meminductor emulator just changing Y2 from resistor to capacitor based on the memristor emulator. In addition, the exciting signal of this circuit is current, so we call the circuit shown in Fig. 2(a) a universal charge-controlled mem-elements emulator. By adding two CCII+s (U5 and U6) and a voltage buffer (U7), we can get the floating type of the emulator as shown in Fig. 2(b). The CCII+'s port properties can be represented by

$$v_X = v_Y, i_Y = 0, i_Z = i_X. \tag{10}$$

The emulator analyses are as follows:

A. Memristor

When Y1 is a resistor R_0 and Y2 is a resistor R_3, the emulator in Fig. 2(a) can represent a memristor. From (10), we can see that all input current $i_{in}(t)$ passes through R_0. So, U1

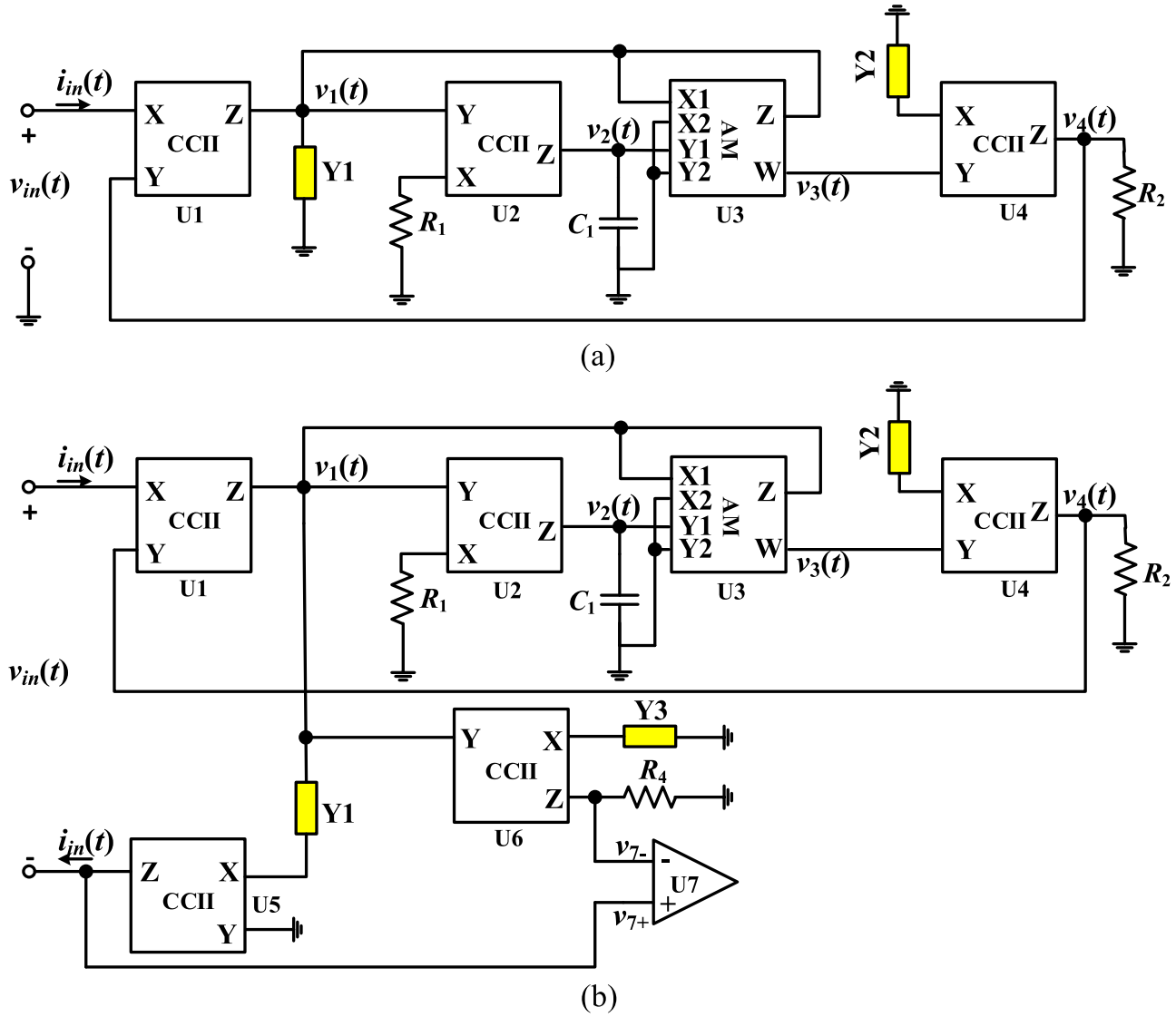


FIG. 2. Universal charge-controlled mem-elements emulator circuit. (a) Grounding type. (b) Floating type.

implements

$$v_1(t) = -i_{in}(t)R_0. \tag{11}$$

U2's terminal X voltage follows the terminal Y, so the current $i_{X2}(t)$ is generated at the x-terminal as follows:

$$i_{X2}(t) = \frac{v_1(t)}{R_1} = -\frac{i_{in}(t)R_0}{R_1} = i_{Z2}(t). \tag{12}$$

U2 and capacitance C_1 constitute integral module to realize

$$v_2(t) = \frac{\int i_{Z2}(t)dt}{C_1} = -\frac{R_0\int i_{in}(t)dt}{R_1C_1} = -\frac{R_0}{R_1C_1}q(t). \tag{13}$$

With the properties of AD633 (used as AM), the output voltage of the U3 is given by

$$v_3(t) = \frac{(V_{X1}-V_{X2})(V_{Y1}-V_{Y2})}{10} + V_Z = \frac{v_1(t)v_2(t)}{10} + v_1(t)$$
$$= -i_{in}(t)R_0 + \frac{{R_0}^2}{10R_1C_1}q(t)i_{in}(t). \tag{14}$$

U4 implements

$$v_4(t) = \frac{R_2}{R_3}v_3(t). \tag{15}$$

Combining (10), (14), and (15), the voltage across the memristor can be written as

$$v_{in}(t) = -\frac{R_0 R_2}{R_3} i_{in}(t) + \frac{{R_0}^2 R_2}{10 R_1 R_3 C_1} q(t) i_{in}(t), \tag{16}$$

which corresponds to (7).

In Fig. 2(b), floating type memristor is constructed when Y3 is a resistor R_5. Here, U5 realizes the transfer of input current, so that the current passing through the memristor remains unchanged. U6 and U7 realize the voltage transfer, and the voltage at the negative terminal of the memristor is as follows:

$$V_- = v_{7+} = v_{7-} = \frac{R_4}{R_5} v_1(t) = -\frac{R_0 R_4}{R_5} i_{in}(t). \tag{17}$$

The voltage at the positive terminal of the memristor is as follows:

$$V_+ = v_4(t) = -\frac{R_0 R_2}{R_3} i_{in}(t) + \frac{{R_0}^2 R_2}{10 R_1 R_3 C_1} q(t) i_{in}(t). \tag{18}$$

So, the voltage across the floating type memristor can be written as

$$v_{in}(t) = V_+ - V_- = \left(\frac{R_0 R_4}{R_5} - \frac{R_0 R_2}{R_3}\right) i_{in}(t) + \frac{{R_0}^2 R_2}{10 R_1 R_3 C_1} q(t) i_{in}(t), \tag{19}$$

which corresponds to (7).

B. Memcapacitor

When we replace resistor R_0 with capacitor C_0, the emulator will convert from memristor to memcapacitor. Here, U1 and capacitance C_0 constitute integral module to implement the integral of the input current by the following formula:

$$v_1(t) = -\frac{\int i_{in}(t) dt}{C_0} = -\frac{q(t)}{C_0}. \tag{20}$$

Similar to the above process of memristor analyses, we can obtain the following relations of memcapacitor:

Grounding type:

$$v_{in}(t) = -\frac{R_2}{R_3 C_0} q(t) + \frac{R_2}{10 R_1 R_3 C_1 C_0} \sigma(t) q(t), \tag{21}$$

Floating type:

$$v_{in}(t) = \left(\frac{R_4}{R_5 C_0} - \frac{R_2}{R_3 C_0}\right) q(t) + \frac{R_2}{10 R_1 R_3 C_1 C_0} \sigma(t) q(t), \tag{22}$$

which both correspond to (8).

C. Meminductor

When we put a resistor R_0 at Y1 and a capacitor C_0 at Y2, the emulator in Fig. 2(a) will be equivalent to a meminductor. Compared with the memristor, U1, U2, and U3 play the same

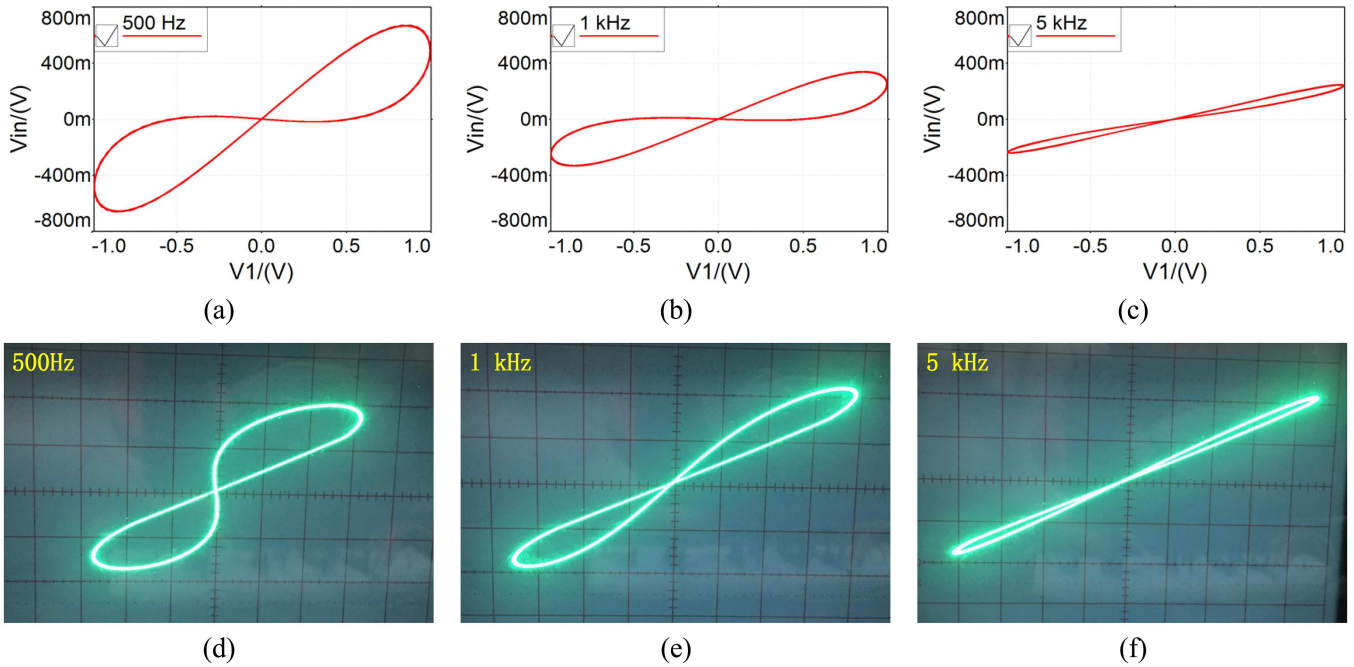


FIG. 3. The *v-i* characteristics of proposed memristor emulator. (a), (b), and (c) are the Multisim circuit simulations with a frequency of 500 Hz, 1 kHz, and 5 kHz, respectively. (d), (e), and (f) are the corresponding circuit experiment results.

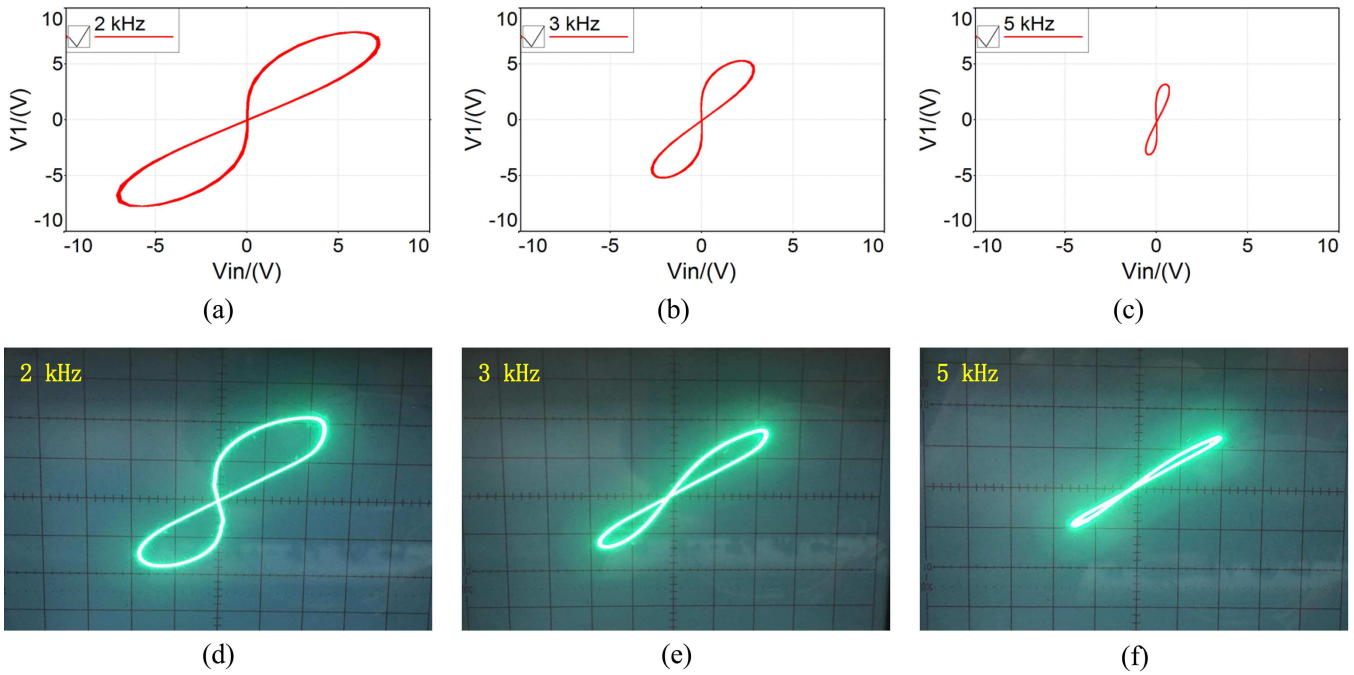


FIG. 4. The *q*-*v* characteristics of proposed memcapacitor emulator. (a), (b), and (c) are the Multisim circuit simulations with a frequency of 2 kHz, 3 kHz, and 5 kHz, respectively. (d), (e), and (f) are the corresponding circuit experiment results.

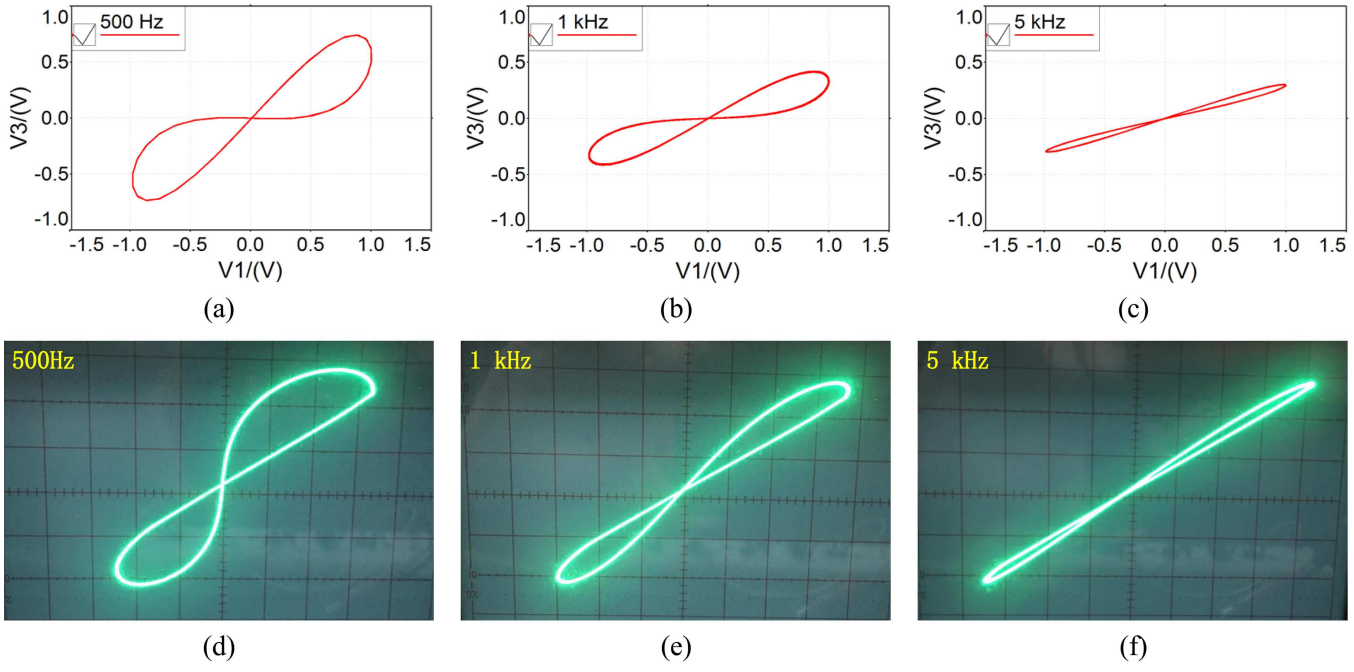
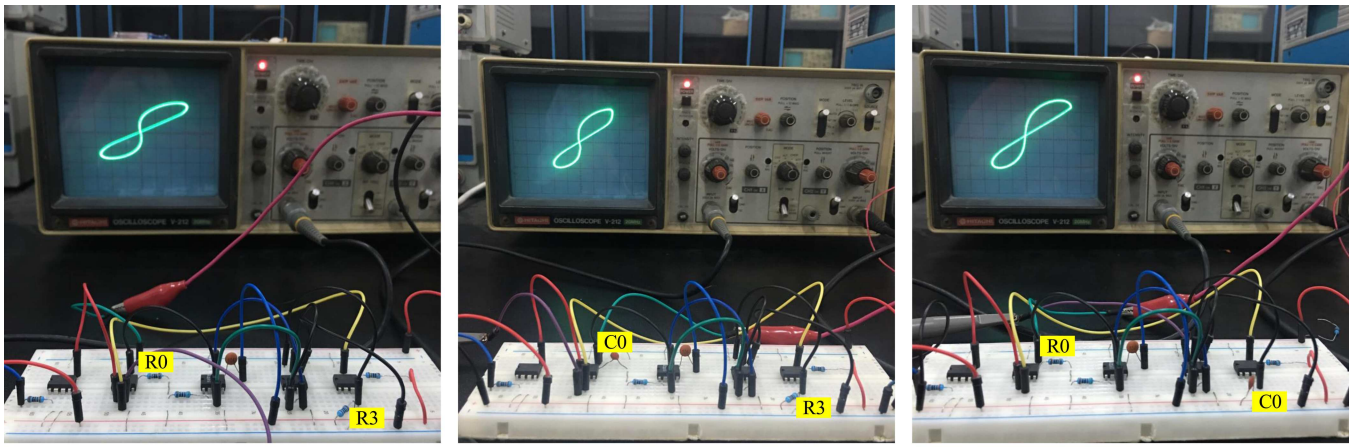


FIG. 5. The φ-*i* characteristics of proposed meminductor emulator. (a), (b), and (c) are the Multisim circuit simulations with a frequency of 500 Hz, 1 kHz, and 5 kHz. (d), (e), and (f) are the corresponding circuit experiment results.



(a) (b) (c)

FIG. 6. The bread board implementation of a proposed universal charge-controlled mem-elements emulator. (a) Memristor. (b) Memcapacitor. (c) Meminductor.

role, only U4 has a different effect, which constitutes a differentiator with C_0. So, we make differential to $v_3(t)$ in (14), the following equation can be obtained:

$$v_{in}(t) = v_4(t) = R_2C_0\frac{d}{dt}\left(-i_{in}(t)R_0 + \frac{{R_0}^2}{10R_1C_1}q(t)i_{in}(t)\right). \quad (23)$$

Since the flux $\varphi(t)$ is defined as $\varphi(t) = \int_0^t v(\tau)d\tau$, (23) can be rewritten as

$$\varphi(t) = -R_0R_2C_0i_{in}(t) + \frac{{R_0}^2R_2C_0}{10R_1C_1}q(t)i_{in}(t), \quad (24)$$

which corresponds to (9).

In Fig. 2(b), floating type meminductor is constructed when Y3 is a capacitor C_2. Here, U6 and C_2 constitute a differential module, and the voltage at the negative terminal of the meminductor is as follows:

$$V_- = v_{7+} = v_{7-} = R_4C_2\frac{dv_1(t)}{dt} = -R_4C_2R_0\frac{di_{in}(t)}{dt}. \quad (25)$$

Therefore, similar to the above analysis process, we can obtain the relationship of a floating type meminductor as follows:

$$\varphi(t) = (R_0R_4C_2 - R_0R_2C_0)i_{in}(t) + \frac{{R_0}^2R_2C_0}{10R_1C_1}q(t)i_{in}(t), \quad (26)$$

which corresponds to (9).

IV. EXPERIMENTAL RESULTS

In order to validate the correctness and performance of the proposed emulator circuit, Multisim simulation software and hardware experiment are used to simulate and analyze the emulator presented in Fig. 2(a). We use AD844 to implement the function of CCII+, which makes the design easier and more direct. Also, integrated chip AD633 is used as AM. Basic features such as the frequency dependence of the pinched hysteresis loop are experimentally discussed in this section.

A. Memristor

The fingerprints of memristor are tested with sinusoidal input current signal. The parameters for implementing the memristor emulator are chosen as follows: $R_0 = R_2 = R_3 = 1\,k\Omega$, $R_1 = 500\,\Omega$, $C_1 = 100\,nF$. When the input terminal is connected to a current source with an amplitude of 1 mA, the results of the Multisim simulation and circuit experiment results are shown in Fig. 3.

In Fig. 3, the frequency dependence of the memristor pinched hysteresis loop is depicted. Note that from Eq. (11), we know $i_{in}(t) = -v_1(t)/R_0$. In order to conveniently measure the current $i_{in}(t)$, we use the voltage $v_1(t)$ substitute the current $i_{in}(t)$, which just take a transformation of $1/R_0$ scale. Figures 3(d)–3(f) show the pinched hysteresis loops of circuit experiment under 500 Hz, 1 kHz, and 5 kHz. They are well consistent with the results of the Multisim simulation shown in Figs. 3(a)–3(c). It is obvious that with the increase of the input

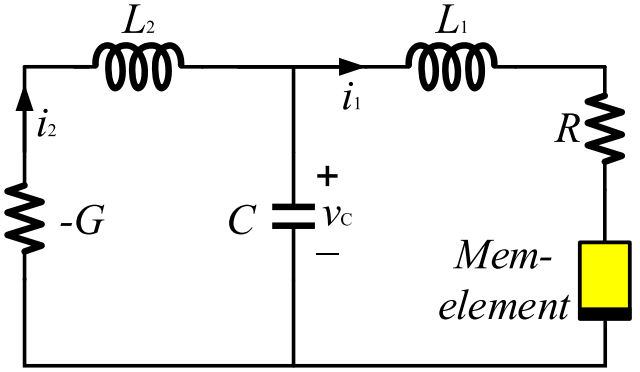


FIG. 7. The universal mem-elements chaotic circuit.

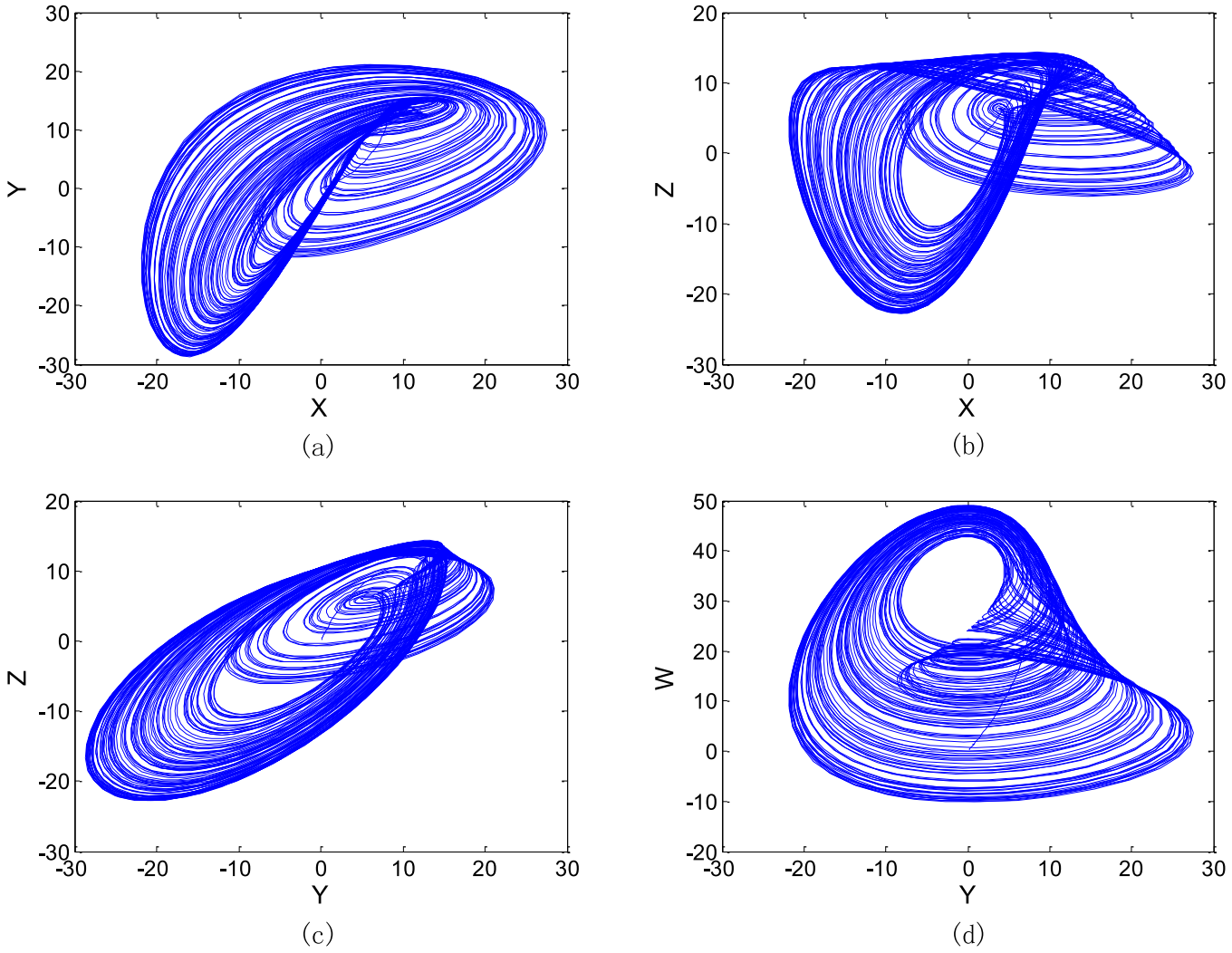


FIG. 8. Phase portraits of proposed memristor system. (a) Projection on *x*–*y* plane. (b) Projection on *x*–*z* plane. (c) Projection on *y*–*z* plane. (d) Projection on *y*–*w* plane.

signal frequency, the area of pinched hysteresis loop gradually decreases and the behavior is close to the linear time-invariant resistor finally, which are consistent with typical memristor fingerprints.[44]

B. Memcapacitor

From (21), we know that the emulator is equivalent to a memcapacitor when replacing resistor R_0 with capacitor C_0. The parameters for implementing the memcapacitor emulator are chosen as follows: $C_0 = 10$ nF, $R_1 = 500\ \Omega$, $R_2 = R_3 = 1$ kΩ, and $C_1 = 100$ nF. When the input terminal is connected to a current source with an amplitude of 1 mA, the Multisim simulation experimental results are shown in Fig. 4. Here, since charge $q(t)$ is relatively small and difficult to be accurately measured, we can use terminal voltage $v_1(t)$ to represent $q(t)$ according to Eq. (20), which just take a transformation of C_0 scale.

Figure 4 depicts the pinched hysteresis loops of memcapacitor at 2 kHz, 3 kHz, and 5 kHz. As the excitation current frequency increases, the pinched hysteresis q-v loops are collapsed owing to the amplitudes of charge and voltage decrease at the same time. This is because the charge is the integral of the input current, which is a function of input frequency f, and the voltage consists of a second harmonic, which is proportional to $1/f$,[3] and a fundamental harmonic, which is proportional to the charge.[32] The circuit experiment results of q-v relationship shown in Figs. 4(d)–4(f) are well consistent with the results of the Multisim simulation shown in Figs. 4(a)–4(c).

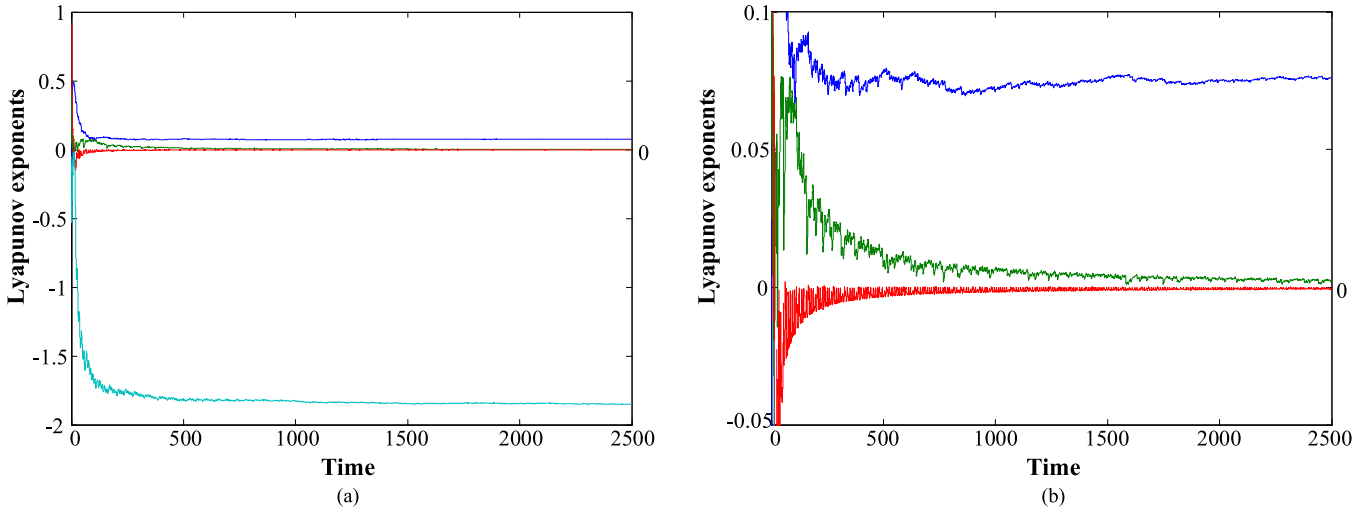


FIG. 9. Lyapunov exponent spectrum of proposed memristor system. (a) Overall. (b) Partial enlargement.

C. Meminductor

Similarly, we know that the emulator is equivalent to a meminductor when Y1 is a resistor R_0 and Y2 is a capacitor C_0. The parameters for implementing the meminductor emulator are chosen as follows: $R_0 = R_2 = 1\,k\Omega$, $R_1 = 500\,\Omega$, $C_1 = 100\,nF$, and $C_0 = 10\,nF$. When the input terminal is connected to a current source with an amplitude of 1 mA, the Multisim simulation experimental results of $\varphi(t)$-$i_{in}(t)$ relationship in different frequencies are shown in Fig. 5.

In Fig. 5, note that from Eq. (23), we know that $v_{in}(t)$ is obtained by differentiating $v_3(t)$, so $v_3(t) = \int_0^t v_{in}(\tau)/(R_2C_0)d\tau = \varphi(t)/(R_2C_0)$ and we use terminal voltage $v_3(t)$ to represent $\varphi(t)$ here. Figures 5(d)–5(f) show the pinched hysteresis loops of circuit experiment under 500 Hz, 1 kHz, and 5 kHz. They are well consistent with the results of the Multisim simulation shown in Figs. 5(a)–5(c). It is obvious that with the increase of the input signal frequency, the area of pinched hysteresis loop gradually decreases and the behavior is close to the linear time-invariant inductor finally.

The bread board implementations of proposed universal charge-controlled mem-elements emulator are shown in Fig. 6.

V. UNIVERSAL MEM-ELEMENTS CHAOTIC CIRCUIT

Based on the models of universal mem-elements in Eqs. (16), (21), and (24), a new chaotic circuit is designed as shown in Fig. 7. This circuit is a deformed structure of Chua's dual circuit.[45] In addition to a resistor and a negative conductance, the circuit also includes 4 dynamic components, which are two inductors, a capacitor, and our proposed mem-elements emulator that is in the yellow block position. The corresponding four state variables are i_1, i_2, v_C, and q, respectively.

By applying Kirchhoff's laws and volt-ampere characteristic of elements to the circuit in Fig. 7, the state equation is described by

$$\begin{cases} L_1\dfrac{di_1}{dt} = v_C - Ri_1 - v_m(q), \\ C\dfrac{dv_C}{dt} = i_2 - i_1, \\ L_2\dfrac{di_2}{dt} = \dfrac{i_2}{G} - v_C, \\ \dfrac{dq}{dt} = i_1, \end{cases} \tag{27}$$

where $v_m(q)$ is the terminal voltage of universal charge-controlled mem-elements emulator we proposed.

When mem-element is a memristor, $v_m(q)$ will be replaced by Eq. (16). Equation (27) becomes

$$\begin{cases} \dfrac{di_1}{dt} = \dfrac{1}{L_1}\left[v_C - Ri_1 - \left(-\dfrac{R_0R_2}{R_3} + \dfrac{{R_0}^2R_2}{10R_1R_3C_1}q\right)i_1\right], \\ \dfrac{dv_C}{dt} = \dfrac{1}{C}(i_2 - i_1), \\ \dfrac{di_2}{dt} = \dfrac{1}{L_2}\left(\dfrac{i_2}{G} - v_C\right), \\ \dfrac{dq}{dt} = i_1. \end{cases} \tag{28}$$

The time scale transformation is carried out and then the dynamic equation of the system is transformed by non-uniform proportional compression. Make $t = L_2d\tau$, $x = i_1$, $y = v_C$, $z = i_2$, $w = q/L_2$, and set parameters for $a = L_2/L_1$, $b = L_2/C$, $c = R$, $k = 1/G$, $m = -R_0R_2/R_3$, and $n = {R_0}^2R_2/R_1R_3C_1$,

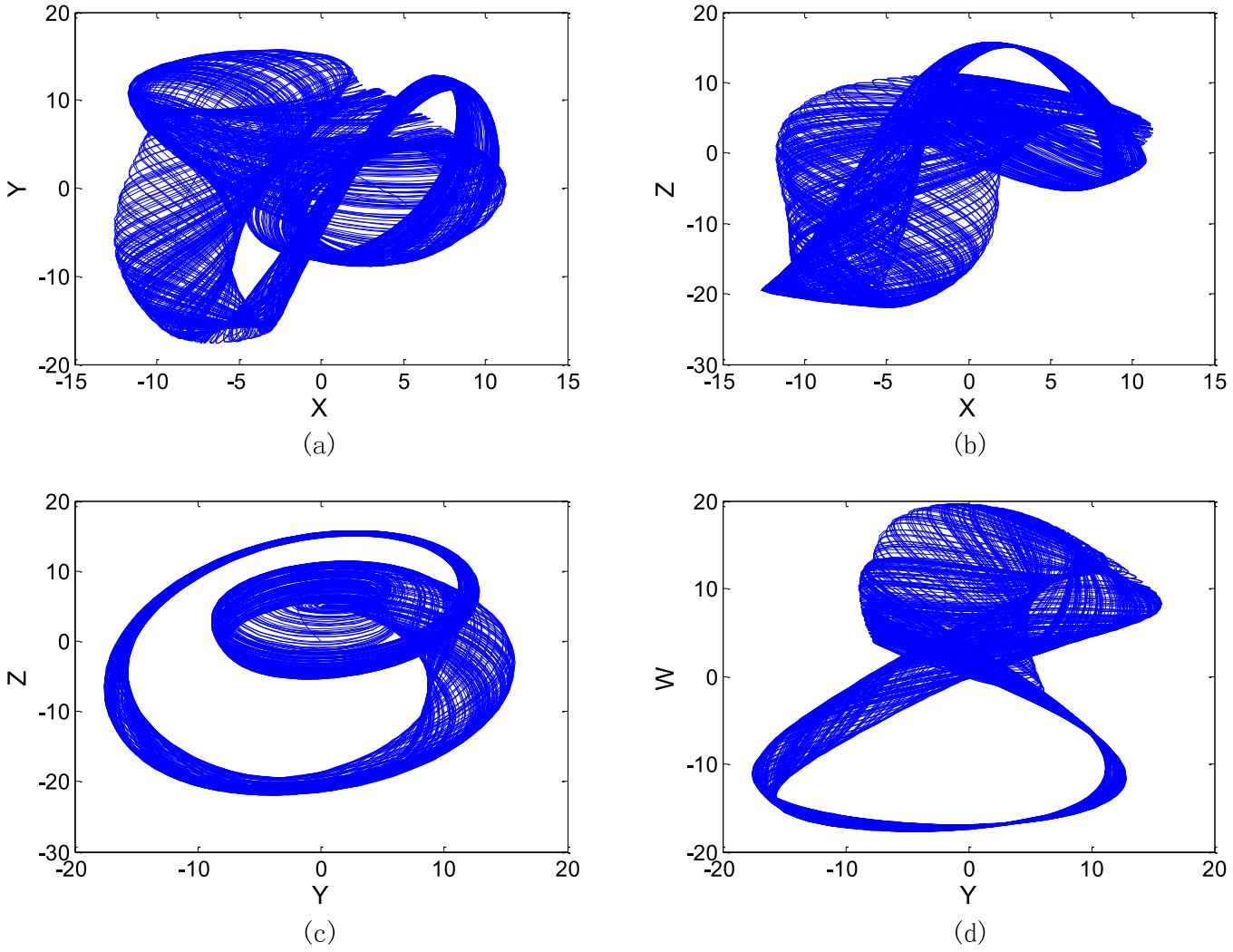


FIG. 10. Phase portraits of proposed memcapacitor system. (a) Projection on *x*–*y* plane. (b) Projection on *x*–*z* plane. (c) Projection on *y*–*z* plane. (d) Projection on *y*–*w* plane.

then the system dynamic equation can be simplified to

$$\begin{cases} \dot{x} = a(y - cx - (m + nw)x), \\ \dot{y} = b(z - x), \\ \dot{z} = kz - y, \\ \dot{w} = x. \end{cases} \tag{29}$$

If we set $a = 2$, $b = 1$, $c = 0.2$, $k = 0.92$, $m = -0.002$, and $n = 0.04$, and give the initial condition (0.01, 0.01, 0.01, 0.01), the chaotic phenomena can be obtained and the phase portraits are shown in Figs. 8(a)–8(d) by solving Eq. (29).

Lyapunov exponents describe motion trajectory mutually exclusive and mutually attractive features which are important for judging a chaotic system. Using the Jacobian method, from Eq. (29) we can obtain the Lyapunov exponent spectrum of system (29) with respect to time t as shown in Fig. 9, and the Lyapunov exponents set which are LE1 = 0.076155, LE2 = 0.002373, LE3 = −0.000399, and LE4 = −1.851722. In Fig. 9, it is clear that there are two positives, one zero, and one negative Lyapunov exponents, which means that the system is a hyper-chaotic system.

When mem-element is a memcapacitor, $v_m(q)$ will be replaced by Eq. (21). Here, in order to be able to solve the set of four differential equations, an equation with respect to σ must be added into Eq. (27), because it has four equations, but

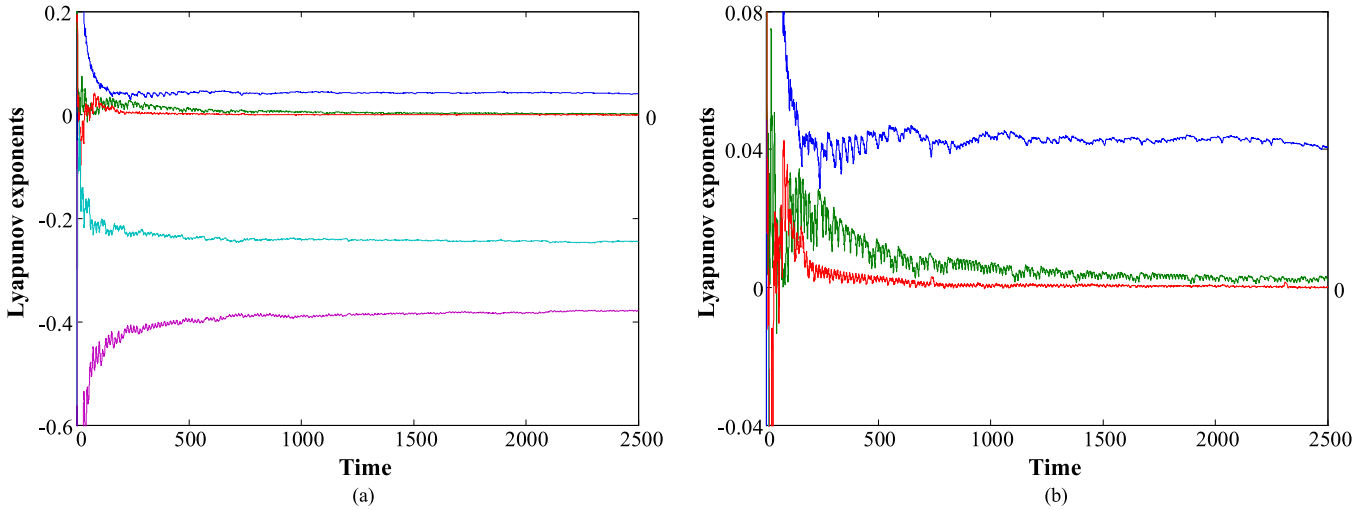


FIG. 11. Lyapunov exponent spectrum of proposed memcapacitor system. (a) Overall. (b) Partial enlargement.

five variables. Therefore, Eq. (27) can be transformed into the following form:

$$\begin{cases} \dfrac{di_1}{dt} = \dfrac{1}{L_1}\left[v_C - Ri_1 - \left(-\dfrac{R_2}{R_3C_0} + \dfrac{R_2}{10R_1R_3C_1C_0}\sigma\right)q\right], \\ \dfrac{dv_C}{dt} = \dfrac{1}{C}(i_2 - i_1), \\ \dfrac{di_2}{dt} = \dfrac{1}{L_2}\left(\dfrac{i_2}{G} - v_C\right), \\ \dfrac{dq}{dt} = i_1, \\ \dfrac{d\sigma}{dt} = q. \end{cases} \tag{30}$$

Make $t = L_2 d\tau$, $x = i_1$, $y = v_C$, $z = i_2$, $w = q/L_2$, $v = \sigma/L_2$ and set parameters for $a = L_2/L_1$, $b = L_2/C$, $c = R$, $k = 1/G$, $m = -R_2/R_3C_0$, and $n = R_2/R_1R_3C_1C_0$, then the system dynamic equation can be simplified to

$$\begin{cases} \dot{x} = a[y - cx - (m + nv)w], \\ \dot{y} = b(z - x), \\ \dot{z} = kz - y, \\ \dot{w} = x, \\ \dot{v} = w. \end{cases} \tag{31}$$

If we set $a = 2$, $b = 1$, $c = 0.38$, $k = 0.18$, $m = -1$, and $n = 0.04$, and give the initial condition (0.01, 0.01, 0.01, 0.01, 0.01), the chaotic phenomena can be obtained as shown in Figs. 10(a)–10(d) by solving Eq. (31).

The Lyapunov exponent spectrum of system (31) versus time t is shown in Fig. 11, and we can obtain the Lyapunov exponents set which are LE1 = 0.040736, LE2 = 0.002191, LE3 = 0.000025, LE4 = −0.244669, and LE5 = −0.378283. In Fig. 10, it is clear that there are two positives, one zero, and two negative Lyapunov exponents, which means that the system is a hyper-chaotic system.

Similarly, when mem-element is a meminductor, $v_m(q)$ will be replaced by Eq. (23). Equation (27) becomes

$$\begin{cases} \dfrac{di_1}{dt} = \dfrac{1}{L_1}\left[v_C - Ri_1 - R_2C_0\dfrac{d}{dt}\left(-i_1R_0 + \dfrac{{R_0}^2}{10R_1C_1}qi_1\right)\right], \\ \dfrac{dv_C}{dt} = \dfrac{1}{C}(i_2 - i_1), \\ \dfrac{di_2}{dt} = \dfrac{1}{L_2}\left(\dfrac{i_2}{G} - v_C\right), \\ \dfrac{dq}{dt} = i_1. \end{cases} \tag{32}$$

Here, since there is a differential form on the right side of the equals sign, we need to simplify the above equation to

$$\begin{cases} \dfrac{di_1}{dt} = \left(v_C - Ri_1 - \dfrac{{R_0}^2R_2C_0}{R_1C_1}{i_1}^2\right)\Big/\left(L_1 - R_0R_2C_0 + \dfrac{{R_0}^2R_2C_0}{10R_1C_1}q\right), \\ \dfrac{dv_C}{dt} = \dfrac{1}{C}(i_2 - i_1), \\ \dfrac{di_2}{dt} = \dfrac{1}{L_2}\left(\dfrac{i_2}{G} - v_C\right), \\ \dfrac{dq}{dt} = i_1. \end{cases} \tag{33}$$

Make $t = L_2 d\tau$, $x = i_1$, $y = v_C$, $z = i_2$, $w = q/L_2$ and set parameters for $a = L_1/L_2$, $b = L_2/C$, $c = R$, $k = 1/G$, $m = -R_0R_2C_0/L_2$, and $n = {R_0}^2R_2C_0/R_1C_1$, then the system dynamic equation can

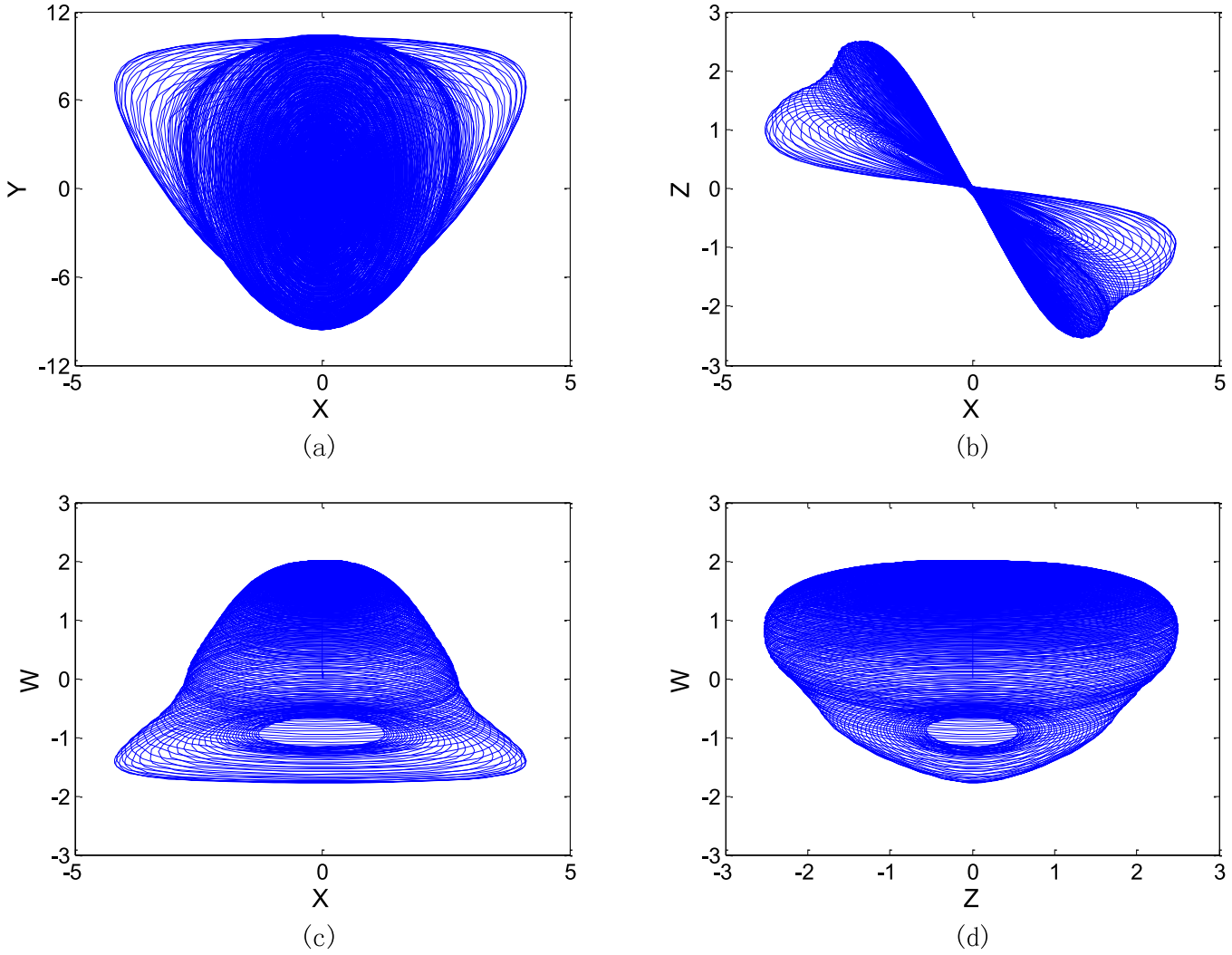


FIG. 12. Phase portraits of proposed meminductor system. (a) Projection on *x*–*y* plane. (b) Projection on *x*–*z* plane. (c) Projection on *x*–*w* plane. (d) Projection on *z*–*w* plane.

be simplified to

$$\begin{cases} \dot{x} = (y - cx - ni^2)/(a + m + nw), \\ \dot{y} = b(z - x), \\ \dot{z} = kz - y, \\ \dot{w} = x. \end{cases} \tag{34}$$

If we set $a=1$, $b=8$, $c=0.04$, $k=0.03$, $m=-0.2$, and $n=0.4$, and give the initial condition (0.01, 0.01, 0.01, 0.01), the chaotic phenomenon can be obtained as shown in Figs. 12(a)–12(d) by solving Eq. (34).

The Lyapunov exponent spectrum of system (34) versus time t is shown in Fig. 13, and we can obtain the Lyapunov exponents set which are LE1 = 0.005257, LE2 = 0.002751, LE3 = −0.000025, and LE4 = −0.008386. It can be seen that there are two positives, one zero, and one negative Lyapunov exponents, which means that the system is a hyper-chaotic system.

VI. CONCLUSION

A compact universal charge-controlled mem-elements emulator capable of producing pinched hysteresis loops behavior has been proposed. Both theoretical analyses and simulation experiments verify the validity of the emulator. The advantage of this universal emulator is that the three mem-elements can be emulated by constructing a simple circuit structure. One of the most attractive advantages is that the

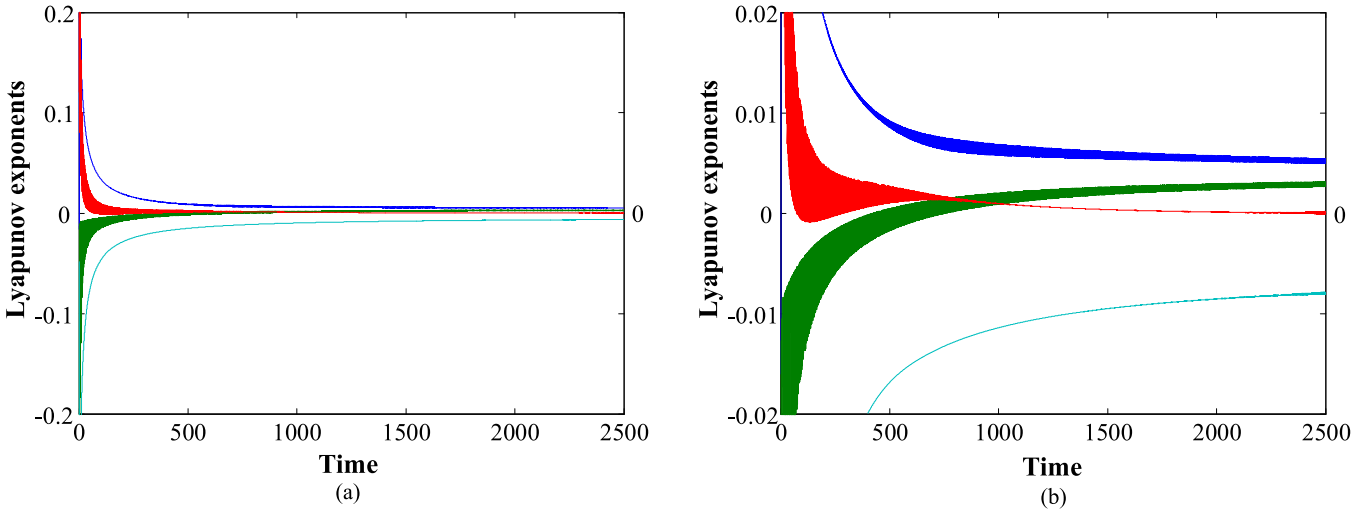


FIG. 13. Lyapunov exponent spectrum of proposed meminductor system. (a) Overall. (b) Partial enlargement.

emulation of memristor, memcapacitor, and meminductor can be implemented by simply replacing a resistor or a capacitor. Our emulator is implemented by common electronic components, so it can be widely applied to the circuit simulation and hardware design of memory devices, providing more flexibility and convenience to researchers. In addition, we also design a novel universal mem-element chaotic circuit, which is characterized by connecting different mem-elements at the same position and then hyper-chaos can be observed by setting the circuit parameters. Such results are convenient for further study of chaotic circuits based on memristor, memcapacitor, and meminductor.

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