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A linearized and low noise CMOS mixer with B-type amplifier-based sub-harmonic balun

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SUMMARY

A low noise and high linearity down-conversion CMOS mixer for 2.4-GHz wireless receiver is presented in this paper. Using a sub-harmonic balun with a simple but effective B-type amplifier, the local oscillator frequency required for this mixer has been reduced by half, and the input local oscillator signal could be single-ended rather than differential, which simultaneously simplifies the design of local oscillator. A distortion and noise cancelation transconductor in association with current bleeding technique is employed to improve the noise and linearity of the entire mixer under a reduced bias current without compromising the voltage gain. Fabricated in a 0.18-μm RF CMOS technology of Global Foundries, the mixer demonstrates a voltage gain of 15.8 dB and input-referred third-order intercept point of 6.6 dBm with a noise figure of 2.6 dB. It consumes 7.65 mA from a 1.0-V supply and occupies a compact area of 0.75×0.71 mm^2 including all test pads.

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KEY WORDS: CMOS mixer; B-type amplifier; sub-harmonic balun; noise cancelation; distortion cancelation

1. INTRODUCTION

In recent years, with evolution of advanced and low-cost CMOS technology, the wireless communication systems are developing rapidly to fulfill the requirements for faster data transmission and higher integration level. Various devices embed wireless communication chips, such as cell phone, laptop, digital TV and camera, to name but a few. There are many wireless transceiver systems that are implemented in direct conversion architecture because of simplified integration and low power consumption. Yet this architecture suffers from the Direct Current (DC) offset problem [1, 2]. Other architectures [3, 4], like the heterodyne transceivers, also have this problem but not as serious as the direct conversion architecture.

The DC offset, caused by self-mixing, is a serious issue in wireless transceivers; it will degrade the performance of the whole transceiver by enlarging the inter-modulation distortion and the noise [5]. The local oscillator (LO) leaking signals are the dominant source of DC offset. The LO signals leak from RF ports of the mixer and traverse to other components like low-noise amplifier (LNA) and filter as a result of incomplete isolation between the RF ports and the LO ports. Besides, they will be reflected back to RF ports of the mixer on account of mismatching among the components and be remixed with LO signals from the local voltage controlled oscillator (VCO), then a DC offset is introduced in the output of the mixer; this is so called the self-mixing. To alleviate this issue, sub-harmonic mixers are proposed, which utilize the second order harmonic of the LO signal in up or

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down converting processes to deal with self-mixing. Even if the leaking LO signal is remixed in the mixer, there will be no DC offset generated. In addition, twice as low LO signal frequency is demanded; the complexity of the LO and synthesizer could be reduced [6].

The mixer is one of the most significant components in transceiver front-end and normally adopts topology of active mixer to achieve better port isolation and higher conversion gain. However, some drawbacks of the active mixer severely affect its performances to the whole transceiver. These drawbacks include big power, large noise, nonlinear distortion and requirements for differential LO input [7–9]. To relieve the large noise and nonlinear distortion problems, a lot of broadband mixers adopt the noise-canceling LNA in the common-source (CS) and common-gate (CG) topology to construct a low-noise transconductor. As demonstrated in [10–12], the LNA-based transconductor allows mixer to obtain a low noise figure (NF) and a high linearity simultaneously without degrading the gain. This paves the way to merge a distortion and noise canceled transconductor into sub-harmonic active mixer in principle.

In this paper, a linearized and low noise CMOS sub-harmonic active mixer is presented utilizing a B-type amplifier-based sub-harmonic balun to overcome the self-mixing phenomenon and simultaneously reduce the number of LO signal input port to one. The distortion and noise canceled transconductor using LNA noise-canceling concept is merged with this mixer and is configured by a current-bleeding technique to decrease the power dissipation of the whole mixer. The mixer works in 2.4 GHz with a desirable noise and distortion performance under a low supply voltage while consumes low power. This paper is organized as follows. Section 2 gives the description of the mixer circuit. Experimental results and comparisons are summarized in Section 3. Finally, conclusions are drawn in Section 4.

2. CIRCUIT DESCRIPTION

2.1. The B-type amplifier-based sub-harmonic balun

Figure 1 shows the circuit topology of the B-type amplifier-based sub-harmonic balun merged into the proposed mixer, and its small signal equivalent circuit is presented in Figure 2.

According to the small signal equivalent circuit, the output voltages of this balun could be separately expressed as:

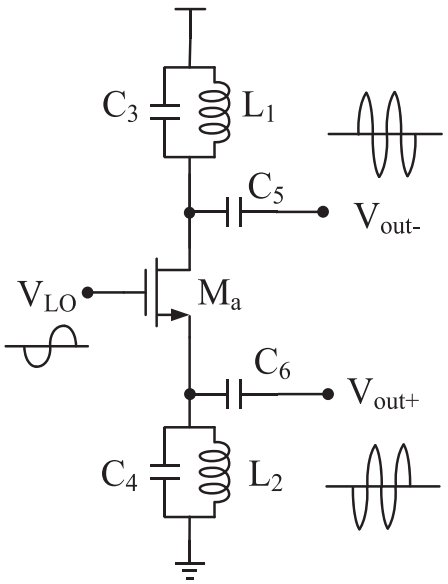

Figure 1. Circuit topology of the b-type amplifier-based sub-harmonic balun.

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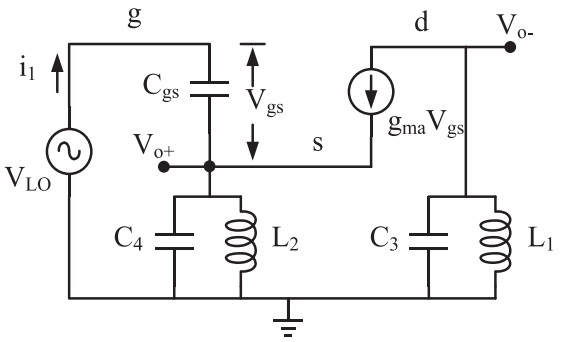

Figure 2. Small signal equivalent circuit of the sub-harmonic balun.

$$V_{O+} = \left(g_{ma}V_{gs} + i_1\right)\frac{1}{sC_4 + 1/(sL_2)} \tag{1}$$

$$V_{O-} = -g_{ma}V_{gs}\frac{1}{sC_3 + 1/(sL_1)} \tag{2}$$

where g_{ma} is the transconductance and V_{gs} is the gate-source voltage of the transistor M_a, respectively.

The current i_1 in equation [1] is the gate current of the transistor M_a. According to the CMOS technology, the gate current is zero in low frequency, and it also will be very small in relatively high frequency. Moreover, the drain current $g_{ma}V_{gs}$ is often much larger than the gate current i_1, and the two currents satisfy:

$$g_{ma}V_{gs} >> i_1. \tag{3}$$

The equation above indicates that the gate current i_1 could be neglected in [1] and [2]. By forcing $L_1 = L_2$ and $C_3 = C_4$, the two output voltages will meet the condition as follow:

$$V_{O+} \approx -V_{O-}. \tag{4}$$

From equation [4], it is clear that the proposed sub-harmonic balun could provide two inverted output voltages with equal magnitude.

Generally, two differentiated LO signals are needed in conventional mixers [13–15]. Comparatively, by using the B-type amplifier sub-harmonic balun in Figure 1, there will be only one LO signal required in this mixer.

Because of the transistor M_a in Figure 1 is working as a B-type amplifier, the input LO voltage (V_{LO}), the drain current (i_d) and the output voltages (V_{o+} and V_{o-}) can be illustrated as in Figure 3.

From Figure 3, it is clear that the drain current of the transistor M_a is a clipped cosine pulse, which could be expressed as:

$$\begin{cases} i_d = i_{d\max}\cos(\omega t) & \left(-\dfrac{\pi}{2} + 2n\pi\right) < \omega t < \left(\dfrac{\pi}{2} + 2n\pi\right) \\ i_d = 0 & otherwise \end{cases}. \tag{5}$$

By expanding the clipped cosine pulse into Fourier series, we can get:

$$i_d = I_{d0} + I_{dm1}\cos(\omega t) + I_{dm2}\cos(2\omega t) + \ldots + I_{dmn}\cos(n\omega t) + \ldots \tag{6}$$

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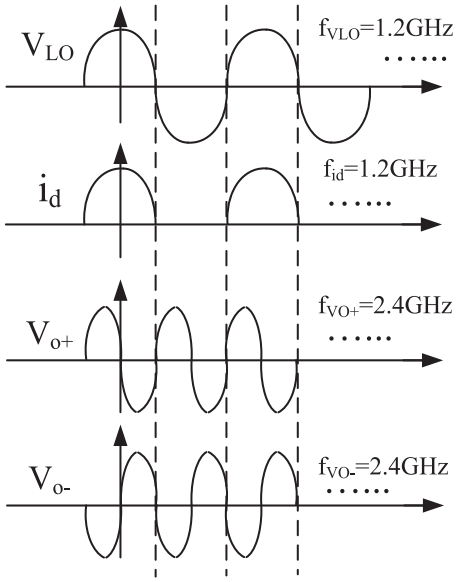

Figure 3. Input voltage, drain current and output voltages of the balun.

$$\begin{cases} I_{d0} = \dfrac{1}{2\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} i_d d_{\omega t} = \dfrac{i_{d\max}}{\pi} \\ I_{dm1} = \dfrac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} i_d \cos(\omega t) d_{\omega t} = \dfrac{i_{d\max}}{2} \\ I_{dm2} = \dfrac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} i_d \cos(2\omega t) d_{\omega t} = \dfrac{2i_{d\max}}{3\pi} \\ \cdots\cdots \\ I_{dmn} = \dfrac{1}{\pi}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} i_d \cos(n\omega t) d_{\omega t} \end{cases} \tag{7}$$

Combining equation [6] with [7], it is obvious that the second harmonic ($2f_{LO}$) of the input voltage is generated as long as the drain current flows through the transistor M_a. However, other order harmonics (f_{LO}, $3f_{LO}$, $4f_{LO}$, $5f_{LO}$, ……, nf_{LO}) will also be generated as well as the second harmonic. Thereby, two LC tanks (L_1, C_3 and L_2, C_4) are configured as band pass filter for the sub-harmonic balun, which are resonated at $2f_{LO}$ and filter out other unexpected harmonics. The output signals of this sub-harmonic balun could be expressed as:

$$\begin{cases} V_{o+} = \dfrac{2i_{d\max}}{3\pi} \cdot \dfrac{L_2}{rC_4} \cos 2\omega t \\ V_{o-} = -\dfrac{2i_{d\max}}{3\pi} \cdot \dfrac{L_1}{rC_3} \cos 2\omega t \end{cases} \tag{8}$$

where r is the parasitic resistance of inductors L_1 and L_2.

Unlike other traditional active mixers, only one LO signal is required in this proposed sub-harmonic mixer, because the B-type amplifier-based sub-harmonic balun can provide two inverted output voltages with equal magnitude. Moreover, the power of LO signals in conventional mixers are relatively large, which increases the VCO complexity. Comparatively, the B-type amplifier-based sub-harmonic balun could amplify the LO signal and then the required LO signal in this sub-harmonic mixer is relatively small, which could simplify the VCO and subsequently reduce the power consumption of the entire wireless receiver.

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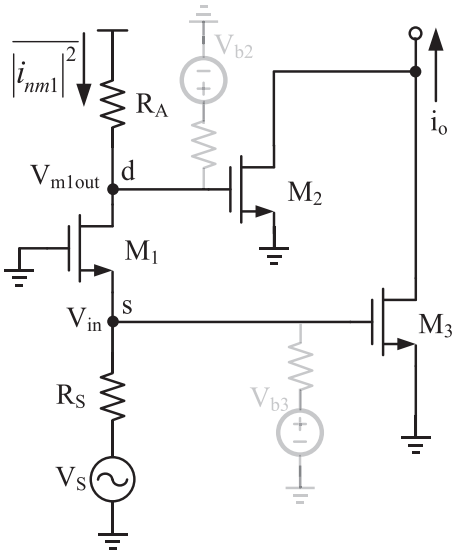

Figure 4. Distortion and noise cancelation transconductor.

2.2. *Distortion and noise cancelation transconductor*

The transconductor of the mixer is displayed in Figure 4. It bases on the noise-canceling LNA topologies used in [16] and essentially influences the linearity and noise performance of the whole mixer. Three transistors (M_1–M_3), which are the main components of the transconductor, transform the RF input voltage into RF currents. The first stage transistor M_1 is configured as a CG amplifier with a distortion and noise cancelation circuit which consists of two transistors (M_2 and M_3) in CS amplifier configuration [17].

According to the basic circuit theory, the transistor M_1 mainly contributes to the NF of whole transconductor. As it works as a CG amplifier, the phase of the input signal voltage will not be changed from source to drain. However, the noise voltage of drain and source will be 180° out-of-phase once the noise current traverses through transistor M_1. When the voltages at drain and source of transistor M_1 are added up by transistors (M_2 and M_3), the signal voltage will be doubled and the noise voltage will be subtracted. Then the noise current from M_1 after being processed by M_2 and M_3 can be expressed as:

$$\overline{|i_{nm1out}|^2} = \overline{|g_{m3}V_{in} - g_{m2}V_{m1out}|^2} = \overline{|i_{nm1}|^2}(g_{m3}R_S - g_{m2}R_A)^2 \tag{9}$$

where $\overline{|i_{nm1}|^2}$ is the total noise current flowing through the transistor and has been marked in Figure 4. To diminish the noise from M_1, [9] should meets the condition that $g_{m3}R_S - g_{m2}R_A = 0$. Thus, the noise from the most noise-contributed component in the transconductor stage of the mixer can be canceled, which includes thermal noise, flicker noise and substrate noise of transistor M_1. However, other noise sources, such as noises from R_A, M_2 and M_3, are not canceled. To get a quantified visualization of the combined impacts from all noise sources, the NF of the entire transconductor should be calculated out. First, the effective transconductance and input impedance of the transconductor are:

$$g_{meff} = g_{m2}\left[\frac{(g_{m1} + g_{mb1})r_{o1} + 1}{r_{o1}/R_A + 1}\right] + g_{m3} \tag{10}$$

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$$Z_{in} \approx \frac{R_A + r_{o1}}{(g_{m1} + g_{mb1})r_{o1} + 1} \tag{11}$$

where g_{mb1} is the M_1's body effect. Moreover, the output noise currents of R_A, M_2, M_3 and the noise at the input from R_S will be expressed as follows:

$$\overline{|i_{nRAout}|^2} = 4kTR_A g_{m2}^2 \tag{12}$$

$$\overline{|i_{nm2out}|^2} = \frac{\gamma}{\alpha} \cdot 4kTg_{m2} \tag{13}$$

$$\overline{|i_{nm3out}|^2} = \frac{\gamma}{\alpha} \cdot 4kTg_{m3} \tag{14}$$

$$\overline{|i_{nRSout}|^2} = \frac{4kT}{R_S} (Z_{in} || R_S)^2 g_{meff} \tag{15}$$

where $\alpha = g_m/g_{d0}$ and γ is the MOSFET noise parameter.

With derivation of all noise currents from each device, the NF of the transconductor can be given by:

$$\begin{aligned} F &= 1 + \frac{\overline{|i_{nRAout}|^2} + \overline{|i_{nm2out}|^2} + \overline{|i_{nm3out}|^2} + \overline{|i_{nm1out}|^2}}{\overline{|i_{nRSout}|^2}} \\ &= 1 + \frac{{g_{m2}}^2 R_A + \frac{\gamma}{\alpha}(g_{m2} + g_{m3})}{\left((Z_{in} || R_S)^2 {g_{meff}}^2\right)/R_S} \\ &+ \frac{\gamma}{\alpha} \frac{\left(g_{m1}(g_{m3}R_S - g_{m2}R_A)^2\right)/((g_{m1} + g_{mb1})R_S + (R_A + R_S)/r_{o1} + 1)^2}{\left((Z_{in} || R_S)^2 {g_{meff}}^2\right)/R_S}. \end{aligned} \tag{16}$$

With the assumption that the input impedance is matched and the noise cancelation condition derived from [9] is well satisfied, equation [16] can be simplified as follow:

$$F = 1 + \frac{R_S}{R_A} + \frac{\gamma}{\alpha}\left(\frac{R_S}{R_A} + 1\right)\frac{1}{g_{m3}R_S}$$

$$when \begin{cases} Z_{in} \approx \dfrac{1}{(g_{m1} + g_{mb1})} = R_S \\ g_{m2}R_A = g_{m3}R_S \end{cases}. \tag{17}$$

According to [17], the NF of the transconductor will be relatively low if the values of R_A and g_{m3} are as large as possible under a constant R_S. Meanwhile, big values of R_A and g_{m3} will actively affect the g_{meff} and consequently achieve a better gain as a result of $A_v = -g_{meff} \cdot R_L$. However, their values cannot be increased immoderately. It is evident in equation [11] that the input impedance is influenced by R_A, and a large g_{m3} with a big gate-source capacitance C_{gsm3} from M_3 will also deteriorate the input matching. The bulk of the CG amplifier is connected to ground for an enhanced body effect, which not only decreases the sensitivity of cancelation circuit to impedance mismatch but also improves the gain of the entire transconductance [18].

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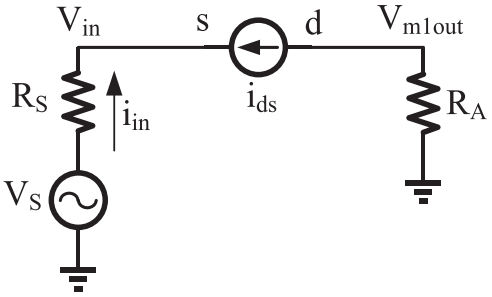

Figure 5. Small signal equivalent circuit model of M_1.

As has been illustrated above, the noise of transistor M_1 can be eliminated by M_2 and M_3. Furthermore, M_1's nonlinear distortion could also be canceled by M_2 and M_3 [19].

The small signal equivalent circuit model of the CG stage (M_1) is displayed in Figure 5, which is utilized to analyze the nonlinear distortion. The nonlinearity of drain current (i_{ds}) is generated by the nonlinear transconductance (g_m) and the nonlinear drain conductance (g_{ds}). The input voltage (V_{in}), which comes from R_S when (i_{ds}) flows through it, is also nonlinear and can be expanded as a Taylor series of the voltage signal source V_S:

$$V_{in} = x_1 \cdot V_S + \left(x_2 \cdot {V_S}^2 + x_3 \cdot {V_S}^3 + \cdots\right) = x_1 \cdot V_S + V_{nl} \tag{18}$$

where the input voltage (V_{in}) is comprised of two blocks, the first-order term part and the high-order terms part (V_{nl}) which includes all unexpected nonlinear terms. The Taylor coefficients are represented by x_n (n = 1,2,3…). The relationship between the input voltage (V_{in}) and the output voltage of the CG stage (V_{m1out}) is given by:

$$\begin{aligned} V_{m1out} &= \frac{R_A}{R_S}(V_S - V_{in}) \\ &= \frac{R_A}{R_S}\left((1 - x_1)V_S - x_2 V_S^2 - x_3 V_S^3\right) \\ &= y_1 V_S + y_2 V_S^2 + y_3 V_S^3 \end{aligned} \tag{19}$$

where $y_1 = (1 - x_1)R_A/R_S$, $y_2 = -x_2 R_A/R_S$, $y_3 = -x_3 R_A/R_S$.

The output current of the entire transconductor ($i_{o,simple}$, it is notable that the output current is deduced by neglecting nonlinear distortion from M_2 and M_3, to get a brief view of the distortion caused by M_1 and simplify the calculation), which is marked in Figure 5, can be derived as:

$$\begin{aligned} i_{o,simple} &= g_{m2} V_{m1out} + g_{m3} V_{in} \\ &= \frac{g_{m2} R_A}{R_S}((1 - x_1)V_S - V_{nl}) + g_{m3}(x_1 V_S + V_{nl}) \\ &= \left(\frac{g_{m2} R_A}{R_S} + x_1\left(g_{m3} - \frac{g_{m2} R_A}{R_S}\right)\right)V_S + \left(g_{m3} - \frac{g_{m2} R_A}{R_S}\right)V_{nl} \end{aligned} \tag{20}$$

where [18] and [19] are used. From [20], it is obvious that the V_{nl} should approximate zero as close as possible to eliminate the nonlinear distortion of transistor M_1 in the output current of the entire transconductor. The nonlinear distortion from M_1 will be perfectly canceled if

$$g_{m3} - \frac{g_{m2} \cdot R_A}{R_S} = 0 \Rightarrow g_{m3} \cdot R_S = g_{m2} \cdot R_A. \tag{21}$$

Equation (21) is identical with noise cancelation condition which has been derived from [9]. In others words, the cancelation circuit cancels the nonlinear distortion of M_1 as well as the noise of M_1 when equation (21) is satisfied. Consequently, the distortion performance of the transconductor

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will mainly be dominated by M_2 and M_3. For a small signal model distortion analysis, the drain current of M_2 and M_3 (i_{ds2} and i_{ds3}) can be denoted by Taylor approximation:

$$i_{ds2} = g_{m2}V_{m1out} + g_{22}V_{m1out}^2 + g_{32}V_{m1out}^3 \tag{22}$$

$$i_{ds3} = g_{m3}V_{in} + g_{23}V_{in}^2 + g_{33}V_{in}^3 \tag{23}$$

where g_{m2} and g_{m3} are the main transconductances of M_2 and M_3, and the second/third order nonlinear coefficients are g_{22}, g_{32}, g_{23} and g_{33}. Then the output current (i_o) without ignoring nonlinear distortion from M_2 and M_3 will be deduced as:

$$\begin{aligned} i_o &= i_{ds2} + i_{ds3} \\ &= g_{m2}V_{m1out} + g_{22}V_{m1out}^2 + g_{32}V_{m1out}^3 \\ &\quad + g_{m3}V_{in} + g_{23}V_{in}^2 + g_{33}V_{in}^3. \end{aligned} \tag{24}$$

Without regard to high-order ingredients (higher than 3), the second-order ($i_{o,2nd}$) and the third-order ($i_{o,3rd}$) expression of the output current are represented by:

$$i_{o,2nd} = (y_2 g_{m2} + x_2 g_{m3})V_S^2 + (y_1 g_{22} + x_1 g_{23})V_S^2 \tag{25}$$

$$\begin{aligned} i_{o,3rd} &= (y_3 g_{m2} + x_3 g_{m3})V_S^3 + \left(y_1^3 g_{32} + x_1^3 g_{33}\right)V_S^3 \\ &\quad + 2(y_1 y_2 g_{22} + x_1 x_2 g_{23})V_S^3. \end{aligned} \tag{26}$$

The first terms of both two expressions above will be truncated by satisfying equation (21), so the nonlinear distortion output current ($i_{o,nl}$) will be:

$$\begin{aligned} i_{o,nl} &= i_{o,2nd} + i_{o,3rd} \\ &= (y_1 g_{22} + x_1 g_{23})V_S^2 + \left[\left(y_1^3 g_{32} + x_1^3 g_{33}\right) + 2(y_1 y_2 g_{22} + x_1 x_2 g_{23})\right]V_S^3. \end{aligned} \tag{27}$$

It is ideal that the $i_{o,nl}$ could be canceled, but the first coefficient $y_1 g_{22} + x_1 g_{23}$ and the second coefficient $\left[\left(y_1^3 g_{32} + x_1^3 g_{33}\right) + 2(y_1 y_2 g_{22} + x_1 x_2 g_{23})\right]$ in (27) cannot be canceled at the same time. On the one side, the nonlinear coefficients g_{22}, g_{32}, g_{23} and g_{33} are obtained by taking the derivative of I_{DS} with respect to the V_{GS}; they are aligned when the gate-source voltage (V_{b2} and V_{b3}) and the W/L scale of transistor M_2 and M_3 are fixed. On the other side, the first item and the second item in (27) have different amplitude characteristics, so they cannot be simultaneously canceled even with the well-design R_A, R_S and nonlinear coefficients. Further analysis in details is proposed in [12] and [19]. Therefore, in our design, the gate-source voltage (V_{b2} and V_{b3}) and the size of components(R_A, R_S, M_2 and M_3) are properly biased and scaled to make the $i_{o,2nd}$ in (27) is reduced and the $i_{o,3rd}$ is canceled.

To get a better design option, two different design cases of the cancelation condition equation (21) are compared and analyzed as follows:

Case 1: The two resistances (R_S and R_A) are identical and the transconductances of transistors M_2 and M_3 are equal, which means $R_S = R_A$ and $g_{m3} = g_{m2}$.
Case 2: The resistance R_A is m times larger than R_S and the transconductance of M_2 is m times smaller than M_3's. Hence it can be expressed as $R_A = m \cdot R_S$ and $g_{m3} = m \cdot g_{m2}$.

Both cases can fulfill the condition equation (21). As has been discussed in [17], relatively large R_A and g_{m3} will decrease their noise contribution and improve performance to the whole transconductor.

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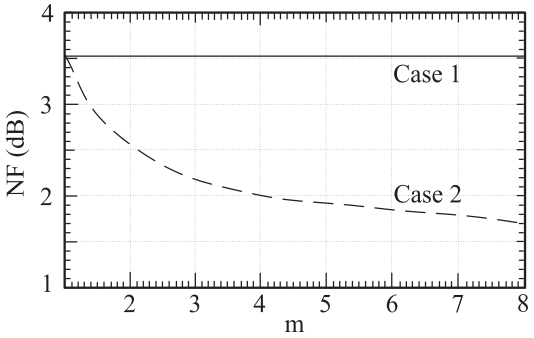

Figure 6. NF versus scaling ratio 'm' for two cases.

Figure 6 shows the NF versus the scaling ratio m under two different cases mentioned above. In case 1, a plotted horizontal line which equals 3.51 dB indicates that the NF is independent on m, while the NF decreases below 3 dB along with increasing of m in case 2. The g_{meff} will also be enhanced as well as the conversion gain in case 2:

$$\begin{aligned} g_{meff,case1} &= g_{m2}\left[\frac{(g_{m1}+g_{mb1})r_{o1}+1}{r_{o1}/R_S+1}+1\right] \\ g_{meff,case2} &= g_{m2}\left[\frac{(g_{m1}+g_{mb1})r_{o1}+1}{r_{o1}/(mR_s)+1}+m\right]. \end{aligned} \tag{28}$$

Furthermore, the equation (21) with a scaling ratio m makes it more convenient to bias the gate-source voltage and change the scale of transistor M_2 and M_3. Utilizing the second and third terms of the third-order expression ($i_{o,3rd}$) for a general demonstration, the residual terms will denoted as:

$$\begin{aligned} i_{o,3rd,term2} &= \left(y_1^3 g_{32}+x_1^3 g_{33}\right)V_S^3 \\ &= \begin{cases} \left((1-x_1)^3 g_{32}+x_1^3 g_{33}\right)V_S^3 \rightarrow case1 \\ \left(m^3(1-x_1)^3 g_{32}+x_1^3 g_{33}\right)V_S^3 \rightarrow case2 \end{cases}. \end{aligned} \tag{29}$$

Comparing case 2 with case 1 in equation (29), it will be more convenient to adjust the size and bias the gate-source voltage of transistor M_2 and M_3 with a scaling ratio m for further optimizing the linearity of the whole transconductor.

2.3. Complete mixer circuit

Figure 7 displays the complete circuit topology of the proposed low noise and high linearity down-conversion CMOS mixer with a B-type amplifier-based sub-harmonic balun. The mixer is generally comprised of three main blocks, which includes the sub-harmonic balun (M_a), the transconductor stage (M_1–M_6) and the switching pairs core (M_7–M_{10}).

The sub-harmonic balun is basically constituted by a B-type amplifier and two LC tanks (C_3, L_1 and C_4, L_2) with single LO signal input terminal. The B-type amplifier functions as a LO frequency-doubling stage and is driven by the LO power. Next to this, the double LC tanks are resonated at the frequency of $2f_{LO}$ and constructed as two band pass filters to filter out other undesirable harmonics generated by the B-type amplifier.

The distortion and noise cancelation transconductor amplifies the received RF signal voltages and converts them into currents. It adopts cancelation circuit to diminish the noise and nonlinear distortion of M_1, which improves the performances of the whole mixer.

The NMOS Gilbert switching pair core is used to modulate the currents provided by the transconductor. Nevertheless, as has been analyzed and discussed in Section 2.2, a relative large M_3 and M_6 are expected for lower noise, which subsequently increases the output current from the

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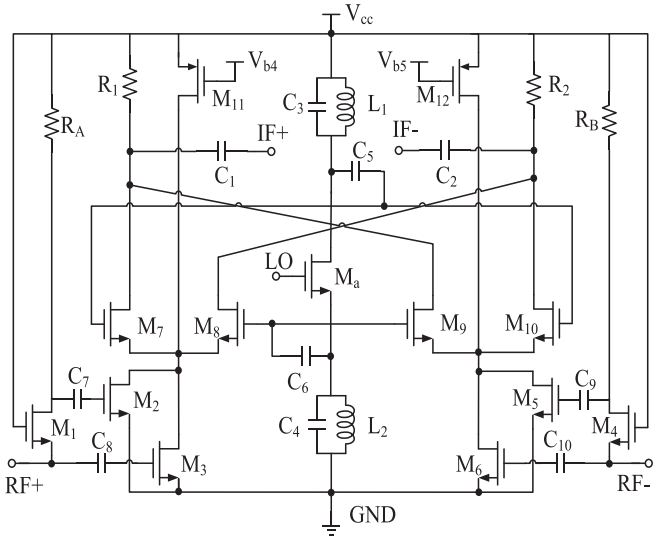

Figure 7. Complete topology of the proposed mixer.

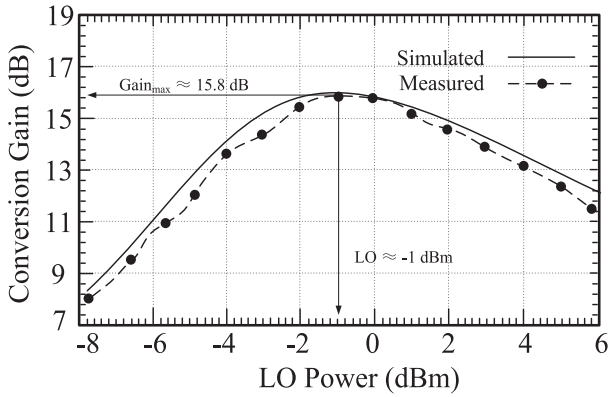

Figure 8. Conversion gain versus LO power.

transconductor. Thus, the switching pair core requires more overdrive headroom to deal with this large current, which enlarges the supply voltage and deteriorates the conversion gain of the mixer. To cope with this issue, the current-bleeding technique (M_{11} and M_{12}) is adopted and injects current to the transconductor, which alleviates the large overdrive voltage requirements of switching pair core to get faster switching speed. In addition, M_{11} and M_{12} increase the size of the load resistors to accomplish even higher conversion gain.

3. MEASURED AND SIMULATED RESULTS

The prototype of this proposed down-conversion mixer is designed and implemented by using the 0.18-μm RF CMOS technology of Global Foundries. Post-layout simulations are realized by Cadence. As the RF port requires fully differential input signals, external hybrids are equipped to transfer the RF signals into anti-phase signals. Besides, the differentiated IF output signals of the mixer are combined into a single-ended signal by an off-chip buffer.

Simulated and measured results of the conversion gain versus LO power are displayed in Figure 8. The gain get a maximum value of almost 15.8 dB when the LO power is around −1 dBm. The measured results of the LO power at RF port and IF port are depicted in Figure 9. The LO leaky

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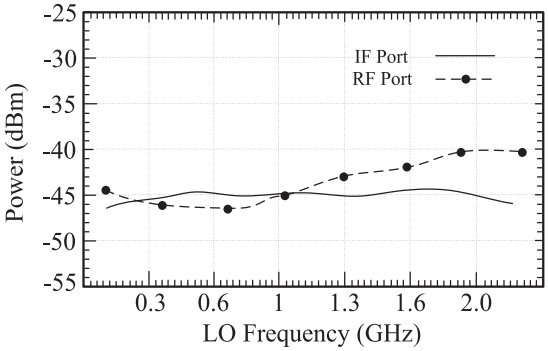

Figure 9. Measured LO power at IF and RF port.

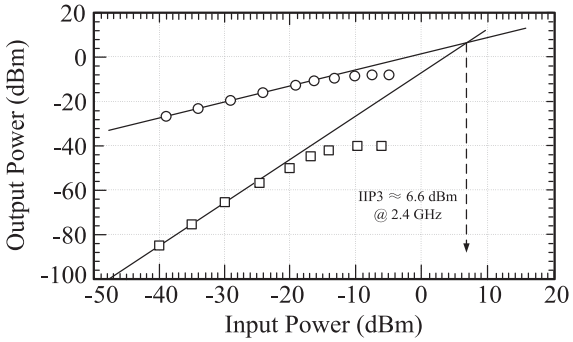

Figure 10. Measured linearity performance of the mixer.

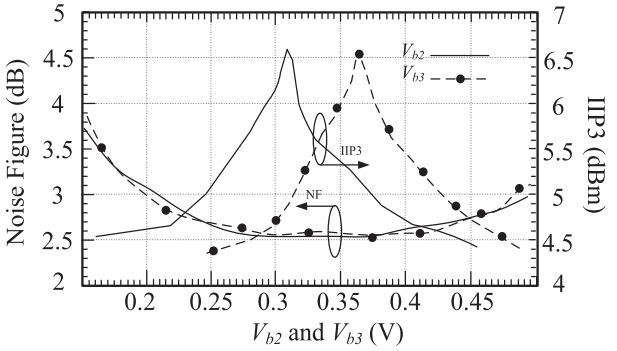

Figure 11. Measured NF and IIP3 sensitivity on V_{b2} and V_{b3}.

power at both ports are less than −40 dBm from 0.3 GHz to 2.0 GHz of LO frequency. Moreover, at the LO frequency of 1.15 GHz, the power at these two ports are around −45 dBm.

Figure 10 is the measured output power versus input power of the mixer on two tones test with 1-MHz spacing. The measured input referred P1dB is about −9.5 dB, while the IIP3 is about 6.6 dBm. The sensitivity of IIP3 and NF on V_{b2} and V_{b3} are testified in Figure 11, to get optimal bias voltages of M_2 and M_3 for [16] and (26).

In Figure 12, the measured NF and IIP3 of the mixer at 2.4 GHz as a function of the supply current are shown. In this figure, the scale of the supply current is checked to make sure that the noise and nonlinear cancelation is appropriately working under a proper supply current. At supply current of

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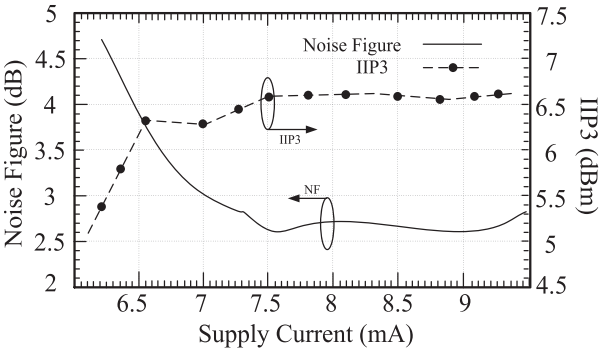

Figure 12. Measured NF and IIP3 of the mixer at 2.4 GHz.

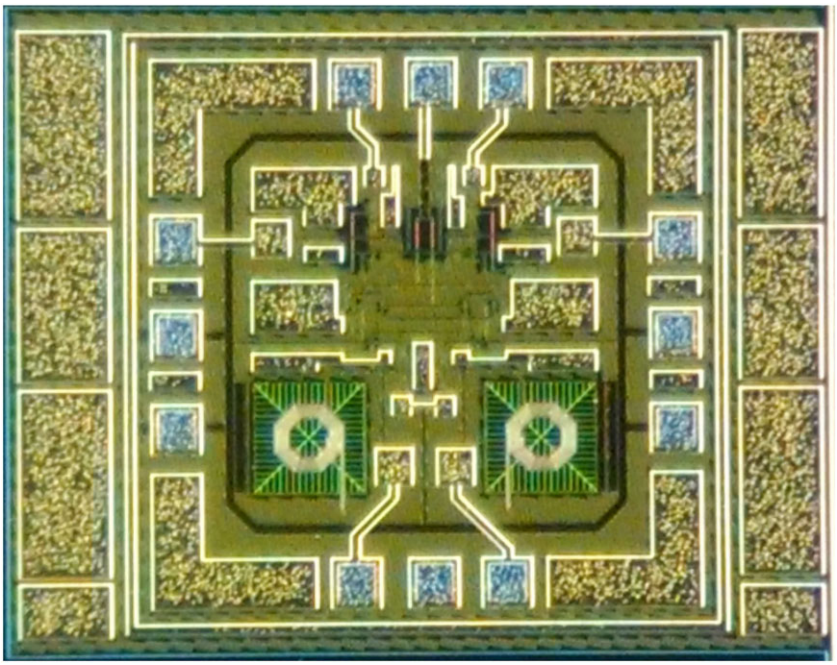

Figure 13. Microphotograph of the mixer.

7.65 mA, the mixer has a IIP3 of 6.6 dBm and a NF of 2.6 dB. The photograph of the testing chip is displayed in Figure 13. As only two inductors are employed in the design, this mixer occupies a compact size of 0.54 mm^2 (750 × 710 μm) including all the dummy blocks and test pads. The core size of the mixer is only about 0.176 mm^2 (470 × 375 μm). The supply voltage of the mixer is 1.0 V, and the power consumption is 7.65 mW.

To validate the robustness, the conversion gain, NF and IIP3 of this proposed mixer versus temperature are simulated under five different corners: Fast–Fast (FF), Fast–Slow (FS), Typical–Typical (TT), Slow–Fast (SF) and Slow–Slow (SS). In Figure 14, the simulated conversion gain results versus temperature for different corners are presented. From the figure, a large conversion gain about 17 dB can be obtained in the FF process under low temperatures condition, and a lower value of 14.3 dB in the worse condition (SS process in high temperatures) is also acceptable. Figure 15 shows the simulated results of NF versus temperature in five corners, and the NF will increase to about 3.8 dB in SS process at high temperature. The IIP3 simulated results versus temperature in five corners, displayed in Figure 16, are more complicated. The IIP3 curves of all five corners are downward parabolas but have different shapes; this phenomenon is mainly caused

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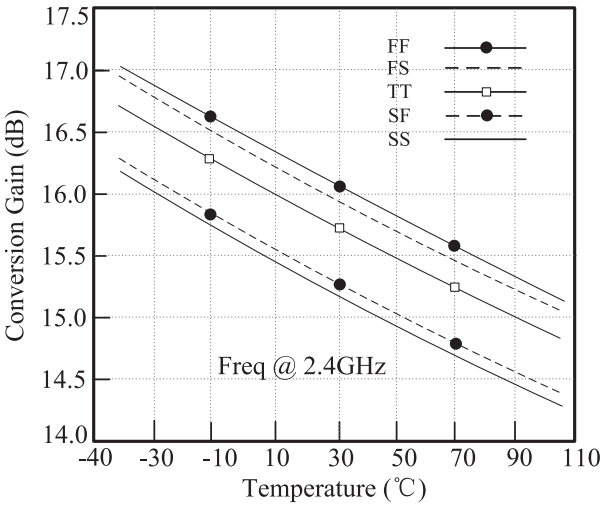

Figure 14. Conversion gain versus temperature in five different corners.

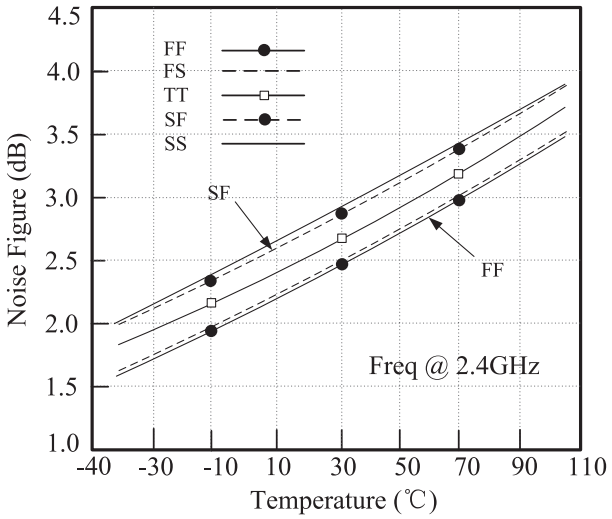

Figure 15. NF versus temperature in five different corners.

by the changing transconductance of the transistors in the mixer and conforms to the theoretical analysis in section 2.2.

Finally, performance of the proposed sub-harmonic mixer is summarized in Table I and illustrated a comparison with other recently reported active mixers. The gain of our mixer is not as good as other mixers while it outperforms other mixers in terms of noise, linearity and chip size occupation with relative low power consumption.

4. CONCLUSIONS

A CMOS sub-harmonic active mixer has presented with improved noise and linearity, utilizing a B-type amplifier-based sub-harmonic balun to overcome the self-mixing phenomenon and simultaneously reduce the number of LO signal input port to one. The distortion and noise canceled transconductor using LNA noise-canceling concept is merged with this mixer and is combined with a current-bleeding technique to decrease the power dissipation of the whole mixer. The mixer

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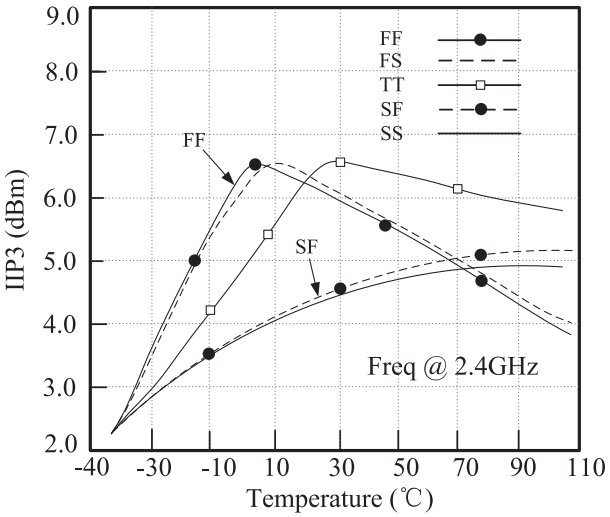

Figure 16. IIP3 versus temperature in five different corners.

Table I. Summary of related works and comparison.

	[8]	[10]	[12]	[14]	[20]	This work
Frequency (GHz)	2.4	1–5.5	0.5–5.8	2.4	2.4	2.4
Technology (nm)	180	130	130	90	90	180
Noise figure (dB)	3	3.9	4.2	16	18	2.6
Supply voltage (V)	1.8	1.5	1.5	0.6	0.5	1.0
Power (mW)	9	34.5	25.5	1	8.5	7.65
Gain(dB)	51	17.5	15	67	30	15.8
IIP3 (dBm)	-30	0.84	2.5	-10.5	-22	6.6
Area (mm^2)	1.2	1	1.2	2.9	3.38	0.54

supplies a conversion gain of 15.8 dB in 2.4 GHz with noise figure of 2.6 dB and IIP3 of 6.6 dBm under a 1-V supply voltage while the power is consuming only 7.65 mW. Comparisons with reported mixers in recent years indicate that our propose mixer is quite suitable for 2.4-GHz ISM-band applications, especially for low noise, higher linearity and low chip size required applications.

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