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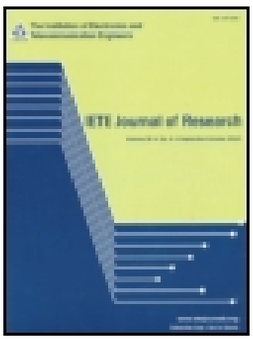

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Systematic Design of Current-Mode Multiple-Loop Feedback Filters Based on a Single CDCTA

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ABSTRACT

In this paper, a new current differencing cascaded transconductance amplifier (CDCTA) is presented. The CDCTA circuit consists of a current differencing unit and *n* cascaded highly linear voltage-controlled transconductance amplifiers, and it possesses wide bandwidth and linear-tunable feature. Based on this CDCTA, a systematic design method generating current-mode (CM) multiple-loop feedback filter is proposed. By altering the parameters of the design matrix, multiple *n*th-order CM all-pole low pass filters structures can be synthesized without changing internal circuit. The *n*th-order filters have low complexity and meet the requirement of no active and passive element matching conditions as adopting only a single CDCTA and *n* grounded capacitors. Furthermore, the frequency of the *n*th-order filters can be linearly tuned by the bias voltage. A fourth-order Butterworth filter is designed as an example, and its Cadence simulation results have good agreement with the theoretical analysis.

KEYWORDS

Current-mode; Filter; Multiple-loop feedback; Wide bandwidth; Linear-tunable feature; CDCTA

1. INTRODUCTION

Compared with voltage-mode circuits, the current-mode (CM) circuits have obvious advantage in analogue and digital signal processors due to their low voltage operation, wide dynamic range, high speed processing, and increased bandwidth. Current differencing transconductance amplifier (CDTA) is one of the most important active building blocks (ABB) in CM signal processing, which has been used in many applications especially in active filters [1–6]. It is really a CM element, whose input and output signals are all current form [7]. Meanwhile, its current input terminals are virtual ground and have no parasitic capacitance, which vastly expands circuit's bandwidth. However, most of reported CDTAs have two main problems: (1) limited bandwidth because of the large input and low output impedance, which is hard to realize the circuit in high frequency; (2) lack of linear-tunable feature, so it is inconvenient to implement linear-tunable filter which can adjust corner frequency linearly and compensate the process errors easily. Additionally, most CDTAs are used for low-order circuit design. The design of high-order CM circuit employs lots of CDTAs [2,3,6]. Undoubtedly, using multiple active components will increase the circuit complexity. Recently, research on high-order CM filter adopting single active device (CDCTA) only in [8] has been reported, the CDCTA in [8] has simple structure, low input impedance, and high output impedance level, etc. However, it is not convenient to design the circuits including negative feedback configurations, thus multiple filter structures realization are not obtainable. In addition, the [8]'s device has no linear-tunable feature. This paper presents a new CDCTA with wide bandwidth and linear-tunable feature to implement multiple filter structures.

Because of the simple structure and high performance, CM active filters have received considerable attention, numerous studies about second-order [1,9–11] and high-order [2,3,12–17] CM active filters have been reported over the last decades. Generally, there are three useful methods for the realization of high-order active filters [18]: (1) cascade connection of second-order sections [2], (2) simulation of passive LC ladder networks [3,12,13], (3) multiple-loop feedback (MF) circuits [14–17]. Cascaded second-order sections have the advantage of simplicity in designing and aligning the filter, however, this method has a high sensitivity. Ladder network adopts a single signal transmission path from source to load, and tends to generate limited transmission zeros, which makes it not general enough. MF active filters have low sensitivity, and arbitrary transmission poles and zeros, so MF is a convenient approach to design high-order filters.

Systematic designs of MF filters are an important method to design multiple filter structures, and it can

find the optimum structure conveniently. In the past few years, several systematic designs of active filters employing MF scheme have been proposed in [11,14–17,19], which use different ABB such as operational transconductance amplifiers (OTAs) in [11,14,15,19], current controlled fully balanced second-generation current conveyor (CFBCCII) in [16], and current feedback operational amplifiers (CFOAs) in [17]. However, these reported circuits based on OTAs, CCs (current conveyors), and CFOAs have serious parasitic effects and limited frequency-bandwidth as well as large power consumption. In addition, these circuits suffer from one or more of the following drawbacks. (1) The circuit has a large number of active and passive components. (2) The frequency of the filters cannot be linearly adjusted. (3) The passive resistance is needed, which is not proper in integrated circuits.

In this paper, a systematic design method producing CM MF filter based on only a single CDCTA is proposed. The CDCTA is a modified version from the CDTA circuit in [20], which has wide frequency-bandwidth and linear-tunable feature. By cascading OTAs in series connection, it can easily achieve *n*th-order integral operation. It simplifies the design of CM filter circuit considerably, especially for the design of high-order filter. Multiple CM all-pole low pass filter structures from systematic design method can be obtained without changing internal circuit. The *n*th-order filters, which adopt only a single CDCTA and *n* grounded capacitors, require no active and passive element matching conditions. Moreover, the frequency of the *n*th-order filters can be linearly tuned by the bias voltage; filters' sensitivity is not more than unity and the effects of the CDCTA non-ideal characteristics are discussed.

2. THE PROPOSED CDCTA AND ITS CIRCUIT REALIZATION

2.1 The Proposed CDCTA

The electrical symbol and behaviour model of the proposed CDCTA are shown in Figure 1(a,b), respectively. The CDCTA has low impedance input terminals p and n, and high impedance output terminals z, x_{iz}, and $-x_i$.

By using the standard notation, this CDCTA can be characterized by the following equations:

$$\begin{cases} V_p = V_n = 0 \\ I_z = I_p - I_n \\ I_{x1z} = I_{x1} = g_{m1} V_z \\ I_{xiz} = I_{xi} = g_{mi} V_{x(i-1)z} = g_{mi} Z_i I_{x(i-1)z}, (2 \le i \le n) \end{cases} \quad (1)$$

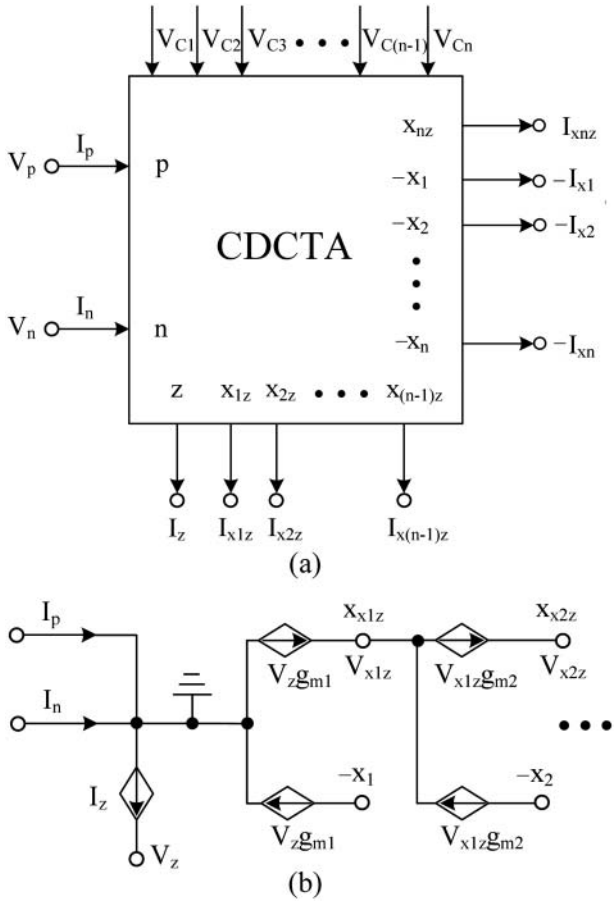

Figure 1: (a) CDCTA electrical symbol and (b) CDCTA behaviour model

where g_{mi} is the transconductance of the ith OTA, which is linearly controllable by external bias voltage V_{Ci}. Z_i is an external impedance connected at the terminal z or $x_{(i-1)z}$. According to Equation (1) and behaviour model of Figure 1(b), the current I_z is the difference current at ports p and n ($I_p - I_n$), and it flows from terminal z into the impedance Z_1. The voltage at the terminal z is transferred into a current I_{x1z} at the terminal x_{1z} by g_{m1}. The voltage at the terminal $x_{(i-1)z}$ is transferred into a current I_{xiz} by g_{mi}. The current at ports x_{iz} and $-x_i$ flows in the opposite direction, but they are equal in magnitude. Additionally, the current at ports $-x_i$ can provide negative feedback current conveniently.

2.2 Its Circuit Realization

The schematic of the CMOS CDCTA circuit is shown in Figure 2. It mainly consists of $n + 1$ fundamental building blocks, namely current differencing unit (CDU) and n cascaded highly linear OTAs. The circuit is simulated by using GlobalFoundries'0.18 μm CMOS process, and it operates under $\pm$0.8 V supply voltage.

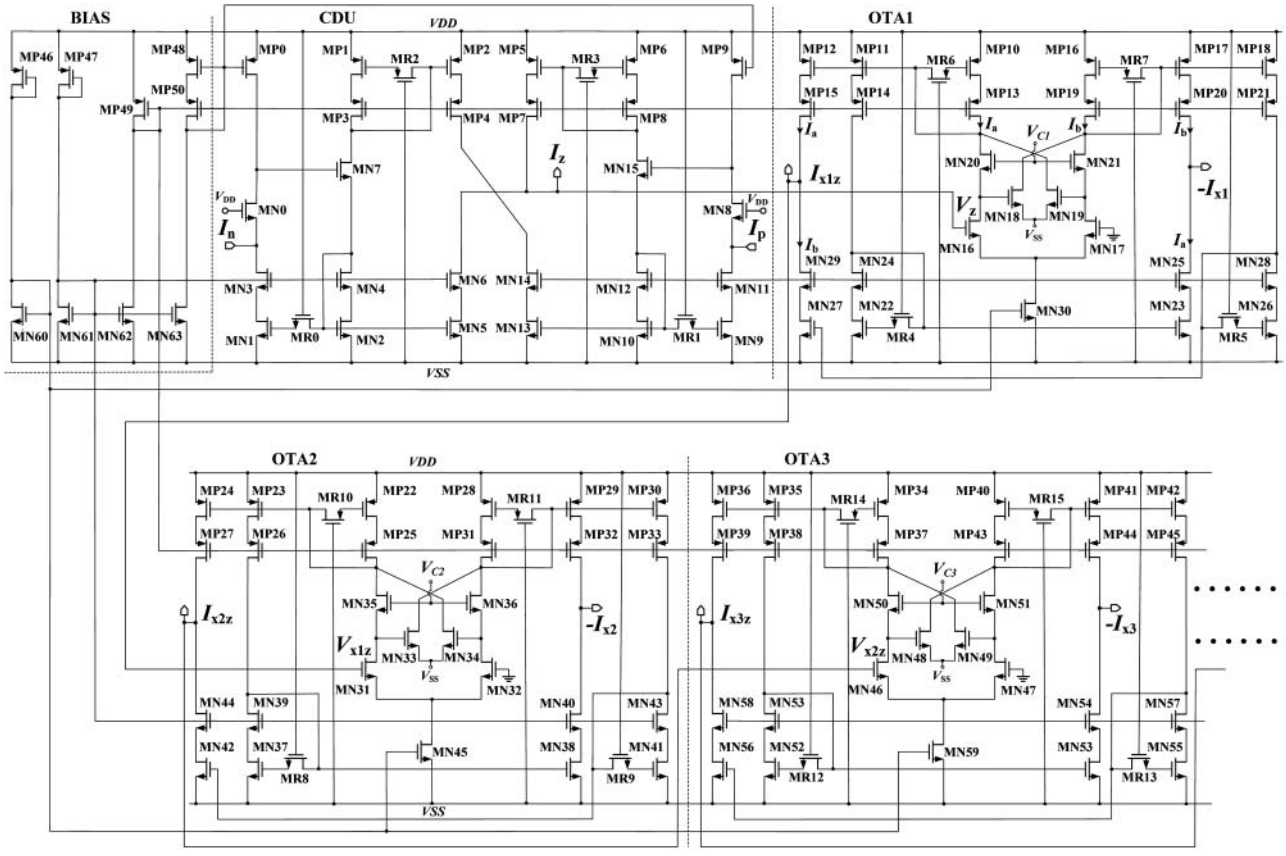

Figure 2: The schematic of the CMOS CDCTA

The CDU, which is a modified version of the compound current conveyor [21], is formed by transistors MN0-MN15 and MP0-MP9. Its current input terminals p and n are virtual ground, which presents low input impedances. Groups of transistors MN1-MN6, MN9-MN14, and MP1-MP8 are low voltage cascaded current mirrors circuits (LVCCMs) which can increase output impedance and produce a precise differential current at the terminal z. Transistors MR0-MR3, which are working in the linear region operate as active compensation resistances, are connected between the gate-to-gate nodes of the transistors to improve whole circuit frequency-bandwidth [22]. Assuming all transistors operate in saturation area and have the same gate length, the input impedance at terminals p, n can be approximated as

$$R_{p,n} = \frac{(g_m + g_{mb})_{MN7,15} + g_{mMN1,9}}{[r_o(g_m + g_{mb})_{MN0,8} + 1](g_m + g_{mb})_{MN7,15} g_{mMN1,9}} \tag{2}$$

where r_o is resistance of MOS transistor between the drain and source, g_m is the transconductance, and g_{mb} is the bulk transconductance.

Since the same relationship between OTA1 and OTAi ($i = 2, 3, \ldots, n$), we analyse the OTA1 as shown in Figure 2. The OTA1 uses a highly linear transconductor in the input section [23]. The linear transconductor circuit was designed by using the MOS linear composite cell (MN16-MN21). Assuming that transistors MN16-MN21 are identical and operate in the saturation region, for simplicity, second-order effects have been neglected, the differential current can be derived as

$$\begin{aligned} I_a - I_b &= (I_{\mathbf{MN20}} - I_{\mathbf{MN18}}) - (I_{\mathbf{MN21}} - I_{\mathbf{MN19}}) \\ &= K(V_{\mathbf{C1}} - V_{\mathbf{SS}} - 2V_{\mathbf{th}})[2V_{\mathbf{GSMN16}} - (V_{\mathbf{C1}} - V_{\mathbf{SS}})] \\ &\quad - K(V_{\mathbf{C1}} - V_{\mathbf{SS}} - 2V_{\mathbf{th}})[2V_{\mathbf{GSMN17}} - (V_{\mathbf{C1}} - V_{\mathbf{SS}})] \end{aligned} \tag{3}$$

where K is transconductance parameter, V_{th} is the threshold voltage, and $V_{\mathrm{C1}} \geq 2V_{\mathrm{th}}$.

The output sections of the OTA1 are LVCCMs through transistor pairs MN22-MN25, MN26-MN29, MP10-MP15, and MP16-MP21. These LVCCMs can also increase output impedance at the x_{1z}, x_1 terminals and accurately copy the input current I_a or I_b, so that the

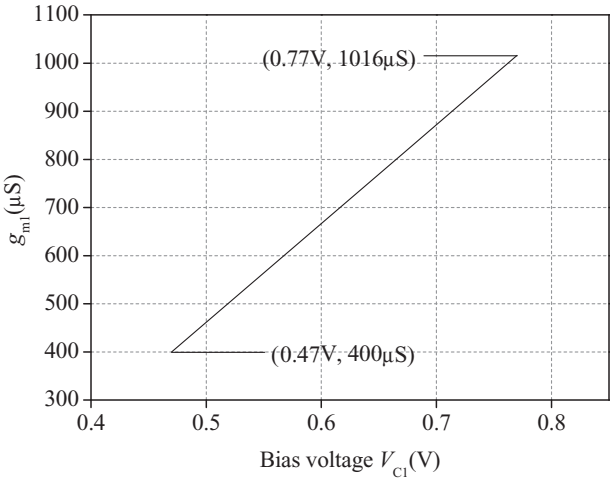

Figure 3: The simulation result of the linear relationship between g_{m1} and V_{C1}

output differential current can be given by

$$I_{x1z} = I_{x1} = I_a - I_b = 2K(V_{C1} - V_{SS} - 2V_{th})V_z = g_{m1}V_z \tag{4}$$

where $-\sqrt{2I_{MN30}/K} \le V_z \le \sqrt{2I_{MN30}/K}$ and $V_z = V_{GSMN16} - V_{GSMN17}$. Equation (4) shows that a highly linear transconductance of $g_{m1} = 2K(V_{C1} - V_{SS} - 2V_{th})$ which is tunable by the bias voltage V_{C1}. In addition, the output sections also use active compensation resistances (MR4-MR7) to enhance frequency-bandwidth.

Figure 3 shows the simulation result of the linear relationship between g_{m1} and V_{C1}, it is clear that the g_{m1} linear variation between 400 and 1016 μS by tuning V_{C1} between 0.47 and 0.77 V.

An effective biasing circuit is designed by transistors MP46-MP50 and MN61-MN64. The biasing circuit provides voltages for transistors that need to be biased by voltage sources.

The output impedance at terminal z can be approximated as

$$R_z = g_{mMP4,7}r_o^2 \| g_{mMN14,6}r_o^2 \tag{5}$$

The output impedance at terminals x_1, x_{1z} can be approximated as

$$R_{x1,x1z} = g_{mMP15,20}r_o^2 \| g_{mMN29,25}r_o^2 \tag{6}$$

The frequency dependence of the input impedances at p and n terminals and the output impedances at z, x_1, and x_{1z} terminals are shown in Figures 4 and 5, respectively. It is known that input impedances at terminals p and n

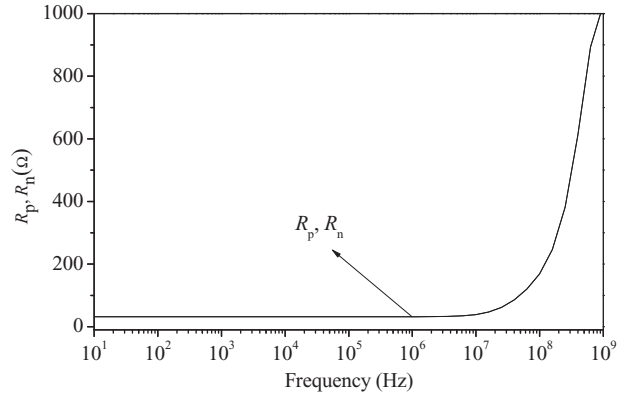

Figure 4: Frequency dependence of the impedance of p and n terminals

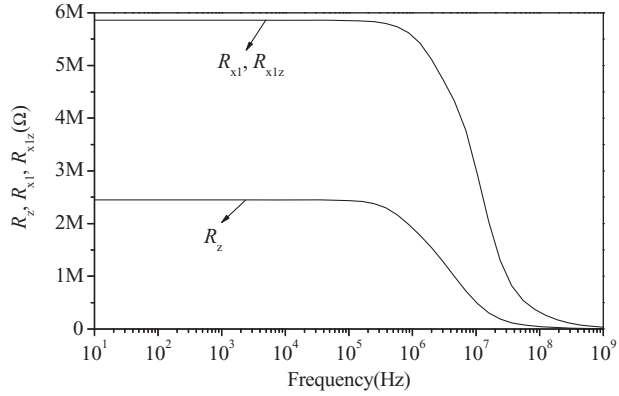

Figure 5: Frequency dependence of the impedance of z, x_1, and x_{1z} terminals

are all 32 Ω when the frequency is below 70 MHz. It can also be seen that output impedances of terminals z, x_1, and x_{1z} are 2.45, 5.86, and 5.86 MΩ, respectively when the frequency is below 1 MHz.

Figure 6 shows the input range of I_p and I_n of CDCTA which proves that the proposed circuit exhibits a very

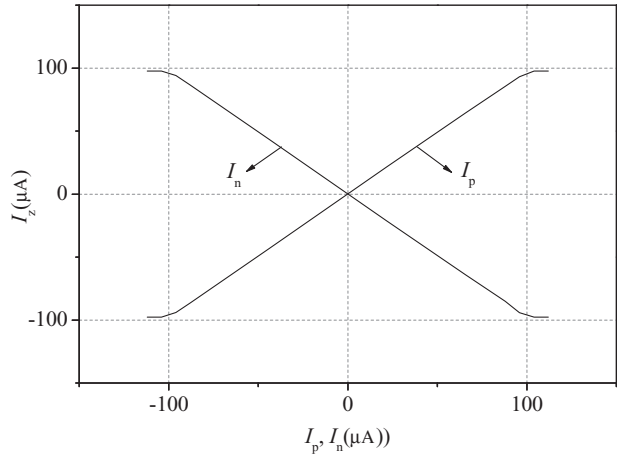

Figure 6: The input range of I_p and I_n of CDCTA, for $V_z = 0$

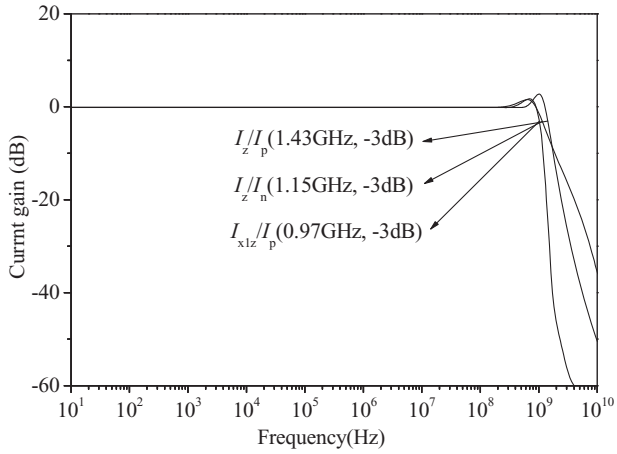

Figure 7: Small-signal transfer characteristics of I_z/I_p, I_z/I_n, and I_{x1z}/I_p (for bias point $I_p = I_n = 0$, $V_{C1} = 0.47$ V, $R_z = 2.5$ K)

good performance (the simulation value of R_z is zero). It is clear that I_z linearly changes in the range of −99–99 μA when I_p or I_n change from −99 to 99 μA. Figure 7 shows the small-signal current transfer characteristics of I_z/I_p, I_z/I_n, and I_{x1z}/I_p. For the bias point $I_p = I_n = 0$, $V_{C1} = 0.47$ V, $R_z = 2.5$ KΩ, the corresponding −3dB bandwidths of small-signal current gains I_z/I_p, I_z/I_n, and I_{x1z}/I_p are 1.43, 1.15, and 0.97 GHz, respectively.

The main performances of the proposed CDCTA and the CDCTA in the reference [8] are compared in Table 1. From Table 1, it is clear that the proposed circuit has the advantages of linear-tunable, wider input range, higher bandwidth, and lower power consumption than the CDCTA in [8] while the input and output impedance characteristics remain in the acceptable range. It is also clear that the proposed circuit (just only contains one OTA) power consumption is 1.79 mW.

To better approximate the real hardware environment, the layout of proposed CDCTA consisting of one CDU

Table 1: Performances comparison between the proposed CDCTA and the CDCTA in reference [8]

Performances	[8]	Proposed CDCTA
Process	0.5 μm MIETEC	GlobalFoundries'0.18 μm
Linear-tunable feature	No	Yes
g_m tunable feature (μS)	0.8–138.4	400–1016
Terminal-*p*, *n* input impedance (Ω)	7.03, 15.18	32
Terminal-*z*, *x*1*z*, *x*1 output impedance ⅀MΩ[a]	3.69, 9.53, 9.53	2.45, 5.86, 5.86
Input range: I_p, I_n (μA)	±30	±99
Bandwidth: I_z/I_p, I_z/I_n, I_{x1z}/I_p (GHz)	0.95, 0.96, 0.93	1.43, 1.15, 0.97
Supply voltage (V)	±1.25	±0.8
Power consumption (mW)[a]	2.48	1.79

[a]When CDCTA just only contains one OTA.

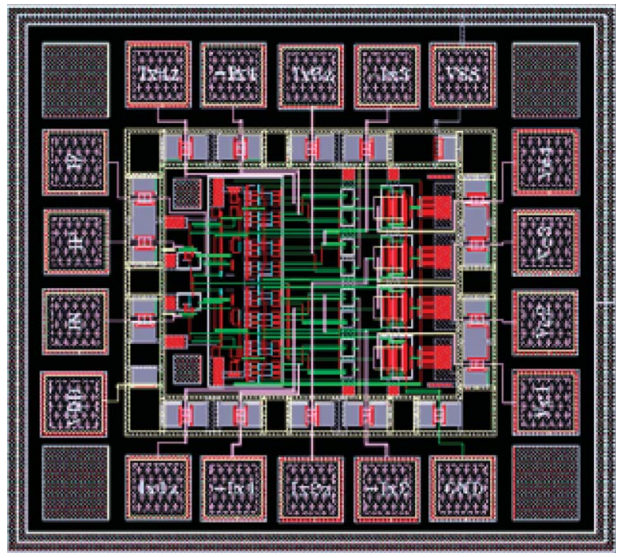

Figure 8: Layout of the proposed CDCTA

and four OTAs has been shown in Figure 8. The total size of the CDCTA layout is 0.75 × 0.65 mm^2. The core size is only 0.4 × 0.35 mm^2.

3. SYSTEMATIC DESIGN OF CM MF FILTERS

3.1 The General Model of Systematic Design

Figure 9 shows the general model circuit of CM MF filter based on a single CDCTA with all capacitors being grounded. This model includes feedforward network consisting of *n* integrators connected in cascade and feedback network that may contain pure wire connections.

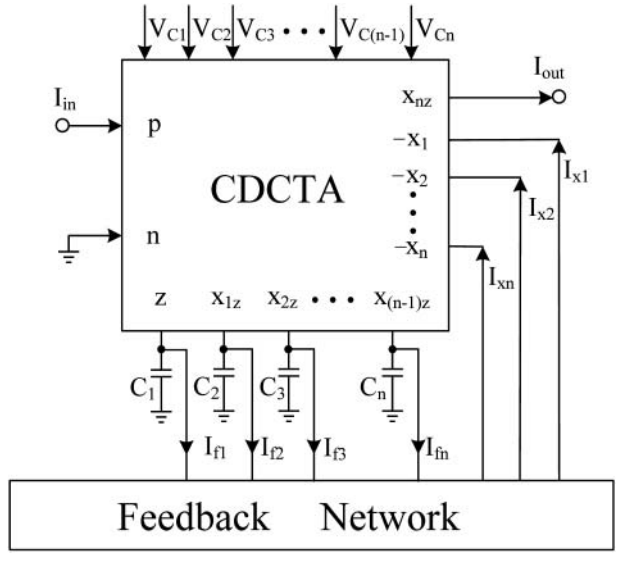

Figure 9: General model circuit of CM MF filter

For convenience of derivation, the feedback network can be written as

$$I_f = FI_x \tag{7}$$

where $I_x = [I_{x1}, I_{x2}, \ldots, I_{xn}]^T$ is the output current vector and $I_f = [I_{f\,1}, I_{f\,2}, \ldots, I_{f\,n}]^T$ is the feedback vector. $F = [f_{ij}]_{n \times n}$ is the feedback coefficient matrix, when $i > j$, $f_{ij} = 0$, so F is an upper triangular matrix, namely:

$$F = \begin{bmatrix} f_{11} & f_{12} & f_{13} & \cdots & f_{1n} \\ 0 & f_{22} & f_{23} & \cdots & f_{2n} \\ 0 & 0 & f_{33} & \cdots & f_{3n} \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & 0 & f_{nn} \end{bmatrix} \tag{8}$$

By inspection, we can write the equations of the feedforward network as

$$\begin{cases} I_{in} - I_{f1} = s\tau_1 I_{x1z} \\ I_{x1z} - I_{f2} = s\tau_2 I_{x2z} \\ I_{x2z} - I_{f3} = s\tau_3 I_{x3z} \\ \quad \cdots \quad \cdots \quad \cdots \\ I_{x(n-1)z} - I_{fn} = s\tau_n I_{xnz} \end{cases} \tag{9}$$

where $\tau_i = C_i/g_{mi}$ is the integrator time constant.

Equation (9) can also be rewritten in a matrix form:

$$I_I - I_f = MI_{xz} \tag{10}$$

where $I_I = [I_{in}, 0, \ldots, 0]^T$, $I_{xz} = [I_{x1z}, I_{x2z}, \ldots, I_{xnz}]^T = I_x$, and

$$M = \begin{bmatrix} s\tau_1 & 0 & 0 & \cdots & 0 \\ -1 & s\tau_2 & 0 & \cdots & 0 \\ 0 & -1 & s\tau_3 & \cdots & 0 \\ \cdots & \cdots & \cdots & \cdots & \cdots \\ 0 & 0 & 0 & -1 & s\tau_n \end{bmatrix} \tag{11}$$

The overall transfer function $H(s)$ of systematic model circuit in Figure 9 can be derived using Equations (7), (8), (10), and (11) as

$$H(s) = \frac{I_{\mathbf{out}}}{I_{in}} = \frac{I_{xnz}}{I_{in}} = \frac{1}{|F+M|} = \frac{1}{|D(s)|} \tag{12}$$

where $|D(s)|$ represents the determinant of $D(s)$.

3.2 All-Pole Filter Generation and Synthesis

The desired general unity DC gain of all-pole low pass transfer functions can be written as

$$H(s) = \frac{1}{b_n s^n + b_{n-1} s^{n-1} + \cdots + b_1 s + 1} \tag{13}$$

A fourth-order Butterworth filter is taken as an example to illustrate the general design theory. As being shown in Figure 9, fourth-order filter is a derivative version corresponding to $n = 4$. Substituting Equations (8) and (11) in Equation (12), the circuit transfer function can be given by

$$\begin{aligned} H(s) = {} & 1/\{(\tau_1\tau_2\tau_3\tau_4)s^4 + (\tau_1\tau_2\tau_3 f_{44} + \tau_1\tau_2\tau_4 f_{33} \\ & + \tau_1\tau_3\tau_4 f_{22} + \tau_2\tau_3\tau_4 f_{11})s^3 + [\tau_1\tau_2(f_{33}f_{44} + f_{34}) \\ & + \tau_1\tau_3 f_{22}f_{44} + \tau_1\tau_4(f_{22}f_{33} + f_{23}) + \tau_2\tau_3 f_{11}f_{44} \\ & + \tau_2\tau_4 f_{11}f_{33} + \tau_3\tau_4(f_{11}f_{22} + f_{12})]s^2 + [\tau_1(f_{22}f_{33}f_{44} \\ & + f_{22}f_{34} + f_{23}f_{44} + f_{24}) + \tau_2(f_{11}f_{33}f_{44} + f_{11}f_{34}) \\ & + \tau_3(f_{11}f_{22}f_{44} + f_{12}f_{44}) + \tau_4(f_{11}f_{22}f_{33} + f_{11}f_{23} \\ & + f_{12}f_{33} + f_{13})]s + (f_{11}f_{22}f_{33}f_{44} + f_{11}f_{22}f_{34} \\ & + f_{11}f_{23}f_{44} + f_{12}f_{33}f_{44} + f_{11}f_{24} + f_{13}f_{44} + f_{12}f_{34} + f_{14})\} \end{aligned} \tag{14}$$

There is a one-to-one correspondence between the matrix F and the circuit structure, different F will produce different circuit structures. Here, we present four practical structures in Figure 10.

The corresponding f_{ij}'s transfer functions and design formulas can be obtained as follows:

Structure 1: $f_{11} = f_{12} = f_{23} = f_{34} = 1$ and others $= 0$

$$\begin{aligned} H(s) = {} & 1/[\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_3\tau_4)s^2 \\ & + (\tau_2 + \tau_4)s + 1] \end{aligned} \tag{15}$$

Comparing Equations (13) and (15), we derive the design formulas:

$$\begin{aligned} & \tau_1 = b_4/b_3,\ \tau_2 = b_3/b,\ \tau_3 = b/(b_1 - b_3/b), \\ & \tau_4 = b_1 - b_3/b,\ b = b_2 - b_1 b_4/b_3. \end{aligned} \tag{16}$$

Structure 2: $f_{14} = f_{24} = f_{34} = f_{44} = 1$ and others $= 0$

$$H(s) = 1/(\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 + \tau_1\tau_2 s^2 + \tau_1 s + 1) \tag{17}$$

Comparing Equations (13) and (17), we derive the design formulas:

$$\tau_1 = b_1,\ \tau_2 = b_2/b_1,\ \tau_3 = b_3/b_2,\ \tau_4 = b_4/b_3. \tag{18}$$

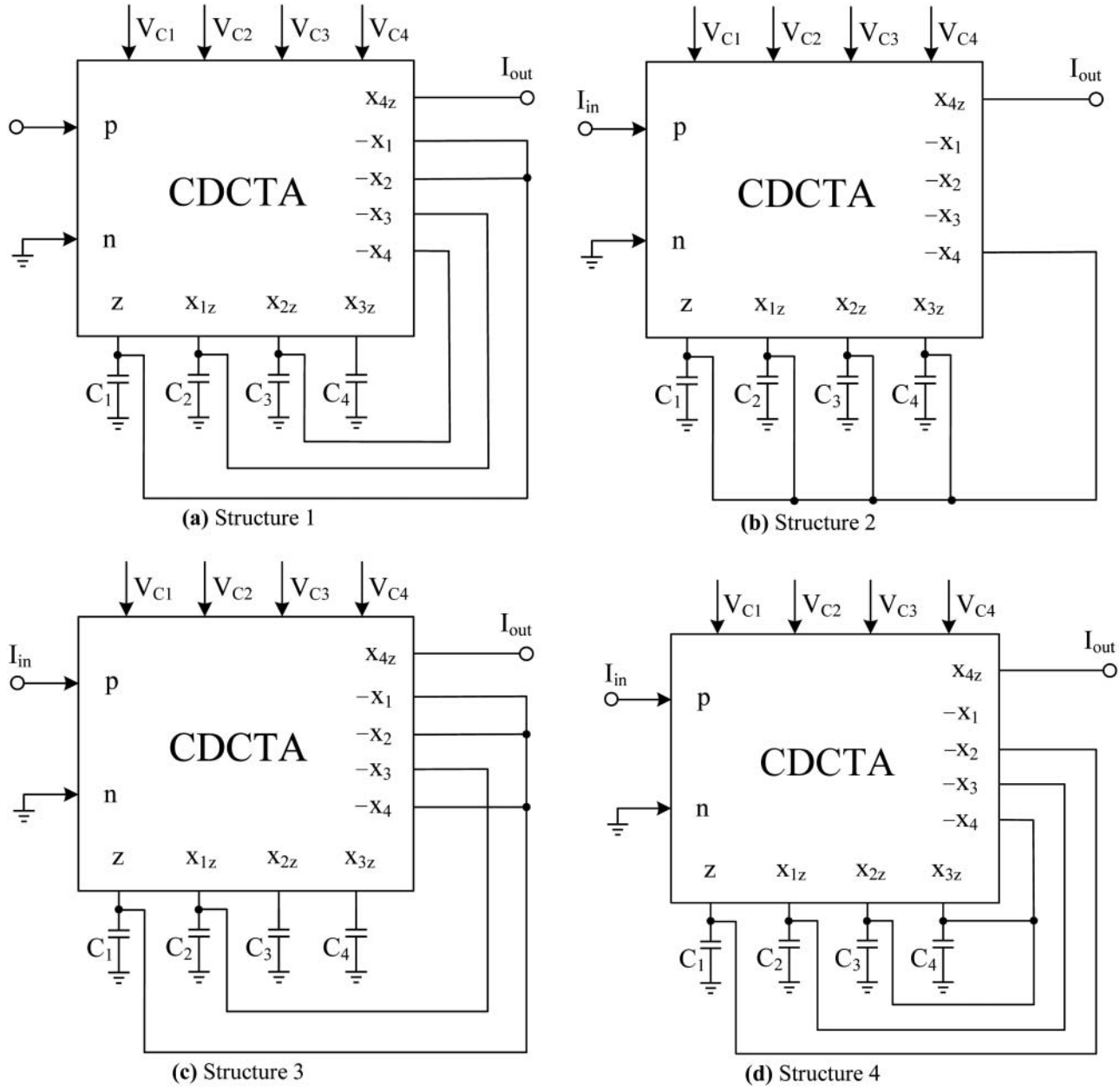

Figure 10: Four structures of CM MF filter

Structure 3: $f_{11} = f_{12} = f_{14} = f_{23} = 1$ and others $= 0$

$$H(s) = 1/[\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_4 + \tau_3\tau_4)s^2 + \tau_4 s + 1] \quad (19)$$

Comparing Equations (13) and (19), we derive the design formulas:

$$\tau_1 = b_4/b_3,\ \tau_2 = b_3/(b_2 - b_1 b_4/b_3),\ \tau_3 = b_2/b_1 - b_4/b_3,\ \tau_4 = b_1. \quad (20)$$

Structure 4: $f_{12} = f_{23} = f_{34} = f_{44} = 1$ and others $= 0$

$$H(s) = 1/[\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_1\tau_2\tau_3 s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_3\tau_4)s^2 + (\tau_1 + \tau_3)s + 1] \quad (21)$$

Comparing Equations (13) and (21), we derive the design formulas:

$$\tau_1 = b_1 - b_3/b,\ \tau_2 = b/(b_1 - b_3/b),\ \tau_3 = b_3/b,\ \tau_4 = b_4/b_3,\ b = b_2 - b_1 b_4/b_3 \quad (22)$$

From the above, the general all-pole low pass CM filter has been presented. It is clear that the structures in Figure 10(a–d) can be easily designed using the attached formulas. When matrix F is chosen so that the elements in the last column all are unity and the other elements of the matrix are zero, the circuit has the inverse follow-the leader-feedback structure, as shown in Figure 10(b).

When the choice is composed of $f_{i(i+1)} = 1$, $i = 1, 2, \ldots, n-1$, $f_{nn} = 1$, $(n = 4)$, and the other f_{ij}'s are zero, then the leap-frog structure results as shown in Figure 10(d).

4. THE EFFECTS OF CDCTA NON-IDEALITIES AND ANALYSIS

4.1 The Effects of CDCTA Non-Idealities

In this section, the effects of CDCTA non-idealities on the proposed filter characteristics will be investigated. For the non-ideal case, the terminal characteristics of the CDCTA in Equation (1) can be rewritten as

$$V_p = V_n = 0,\ I_z = \alpha_p I_p - \alpha_n I_n,\ I_{x1z} = I_{x1} = \beta_1 g_{m1} V_z,$$
$$I_{xiz} = I_{xi} = \beta_i g_{mi} Z_i I_{x(i-1)z},\ (2 \le i \le n) \quad (23)$$

where α_p and α_n are parasitic current gains between $p-z$ and $n-z$ terminals, β_1 and β_i are the transconductance inaccuracy factors between $z-x_1$ and $x_{(i-1)z}-x_{iz}$ terminals, respectively. These transfer gains α_p, α_n, β_1, and β_i slightly deviate from ideal unit values by the effect of the CDCTA tracking errors.

Figure 11 shows the simplified equivalent circuit that will be used to represent the model of non-ideal CDCTA. There are two parasitic resistors (R_p and R_n) at the input terminals p and n, parasitic resistors, and capacitors from the terminals z, x_{iz}, and x_i to the ground ($R_z \,||\, C_z$, $R_{xiz} \,||\, C_{xiz}$ and $R_{xi} \,||\, C_{xi}$), respectively. Here, $R_{xiz} = R_{xi} = R_x$ and $C_{xiz} = C_{xi} = C_x$. Therefore, taking into account the CDCTA parasitics with $\alpha_p = \alpha_n = \beta_1 = \beta_i = 1$, the operation frequency range for proposed filters can be considered.

For example, we consider the circuit in Figure 10(a), where the grounded capacitors C_1, C_2, C_3, C_4 are connected at the z, x_{1z}, x_{2z}, x_{3z} terminals, there is a low-frequency limitation due to the capacitors C_1, C_2, C_3, C_4, and the parasitics at the terminals z, x_{1z}, x_{2z}, x_{3z}, respectively. The z terminal is connected with two x terminals, the x_{1z} terminal is connected with a single x terminal, and the x_{2z} terminal is also connected with a single x terminal, namely, the impedances at the$z$, x_{1z}, x_{2z}, x_{3z} terminals are $R_z \,||\, R_x \,||\, R_x \,||\, (C_z + 2C_x + C_1)$, $R_x \,||\, R_x \,||\, (2C_x + C_2)$, $R_x \,||\, R_x \,||\, (2C_x + C_3)$, $R_x \,||\, (C_x + C_4)$, respectively. The low-frequency range operation of this filter can thus be approximated to

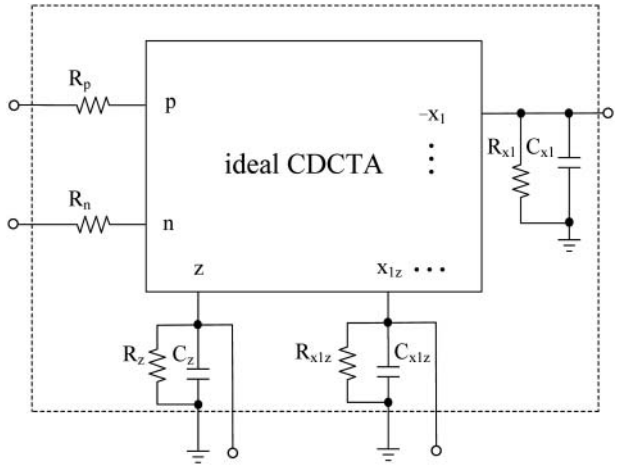

Figure 11: Simplified equivalent circuit of the non-ideal CDCTA

$$f \ge \frac{1}{2\pi R_z \,||\, R_x \,||\, R_x \,||\, (C_z + 2C_x + C_1)} = \frac{1}{\pi R_z \,||\, R_x \,||\, (C_z + 2C_x + C_1)} = f_{L1} \quad (24)$$

$$f \ge \frac{1}{2\pi R_x \,||\, R_x \,||\, (2C_x + C_2)} = \frac{1}{\pi R_x \,||\, (2C_x + C_2)} = f_{L2} \quad (25)$$

$$f \ge \frac{1}{2\pi R_x \,||\, R_x \,||\, (2C_x + C_3)} = \frac{1}{\pi R_x \,||\, (2C_x + C_3)} = f_{L3} \quad (26)$$

$$f \ge \frac{1}{2\pi R_x (C_x + C_4)} = f_{L4} \quad (27)$$

Meanwhile, assume that a load resistor R_L is connected at the output terminal x, the high-frequency range of operation is limited by R_L and a parallel impedance $R_x \,||\, C_x$ at the terminal x. In the practical design, the parasitic resistance R_x is much greater than R_L ($R_x \gg R_L$), the parasitic capacitor C_x is far less than grounded capacitor C_i ($C_x \ll C_i$). So, the high frequency limitation of the filter can be restricted by

$$f \le \frac{1}{2\pi R_L \,||\, R_x \,||\, C_x} \approx \frac{1}{2\pi R_L C_x} = f_H \quad (28)$$

Therefore, according to Equations (24)–(28), the effects of CDCTA non-idealities on the circuit in Figure 10(a) can be ignored as long as the operating frequency f of filter is restricted to the following condition [24]:

$$10 \times \max\{f_{L1}, f_{L2}, f_{L3}, f_{L4}\} \le f \le 0.1 \times f_H \quad (29)$$

4.2 Sensitivity Analysis

Sensitivity is an important criteria in assessing the active filter quality. Here, two ways for analysing the sensitivity of filter can be considered.

Way (1): By calculating the τ_i sensitivity, we can further calculate the sensitivities of the C_i and g_{mi} using the $\tau_i = C_i/g_{mi}$, so we only consider about the τ_i sensitivity. From Equation (15), the sensitivities of filter in Figure 10(a) can be expressed as follows:

$$S_{\tau_1}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + (\tau_1\tau_2 + \tau_1\tau_4)s^2}{F(s)}, \tag{30}$$

$$S_{\tau_2}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_1\tau_2 s^2 + \tau_2 s}{F(s)}, \tag{31}$$

$$S_{\tau_3}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + \tau_3\tau_4 s^2}{F(s)}, \tag{32}$$

$$S_{\tau_4}^{H(s)} = \frac{\tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_4 + \tau_3\tau_4)s^2 + \tau_4 s}{F(s)}, \tag{33}$$

where $F(s) = \tau_1\tau_2\tau_3\tau_4 s^4 + \tau_2\tau_3\tau_4 s^3 + (\tau_1\tau_2 + \tau_1\tau_4 + \tau_3\tau_4)s^2 + (\tau_2 + \tau_4)s + 1$. Figure 12 illustrates the simulation result, the sensitivities of $\boldsymbol{\tau}_i$ are very close to each other, and they are found to be not more than unity in magnitude.

Way (2): After considering the effects of CDCTA non-idealities, transfer function of the filter in Figure 10(a) can be rewritten as follows:

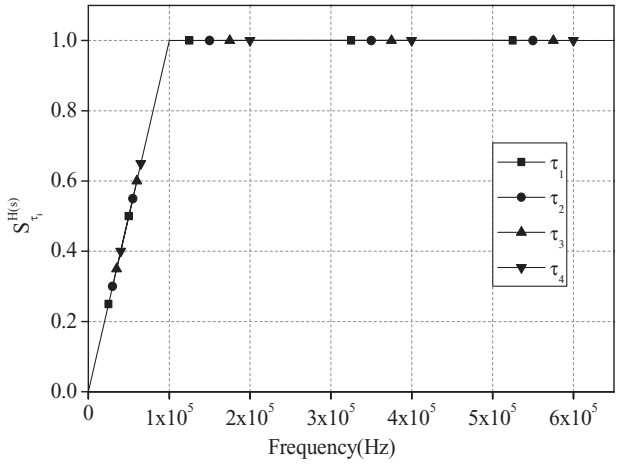

Figure 12: The sensitivities of fourth-order Butterworth LF filter in Figure 10(a)

$$H'(s) = \frac{\alpha_p}{a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + 1} \tag{34}$$

where $a_4 = C_1C_2C_3C_4/(\beta_1\beta_2\beta_3\beta_4{}^* g_{m1}g_{m2}g_{m3}g_{m4})$, $a_3 = C_2C_3C_4/(\beta_2\beta_3\beta_4{}^* g_{m2}g_{m3}g_{m4})$, $a_2 = C_1C_2/(\beta_1\beta_2{}^* g_{m1}g_{m2}) + C_1C_4/(\beta_1\beta_4{}^* g_{m1}g_{m4}) + C_3C_4/(\beta_3\beta_4{}^* g_{m3}g_{m4})$, $a_1 = C_2/(\beta_2{}^* g_{m2}) + C_4/(\beta_4{}^* g_{m4})$.

The sensitivities of filter to the variations in the active components can be derived as $S_{\alpha_p}^{H'(s)} = 1, S_{\alpha_n}^{H'(s)} = 0, S_{\beta_i}^{H'(s)} < 1$. The sensitivities of filter to the variations in the passive elements can also be derived as $S_{g_{mi}}^{H'(s)} < 1, S_{C_i}^{H'(s)} > -1$. It is clear that the sensitivity to active or passive component variation is all less than unit; hence, the proposed filter has a good sensitivity performance.

4.3 Noise Analysis

The noise performance of the active element CDCTA is significant to the implementation of filter. To the basic CMOS active devices, the main noise sources are thermal noise and flicker noise; the flicker noise is often negligible due to the high-frequency operation of the CDCTA. The thermal noise of MOS transistors can be regarded as a current source which is between the drain and source of transistors [25]. The transistors operate in saturation area with the spectral density of thermal noise:

$$\overline{i_n^2} = 4kT\gamma g_m \tag{35}$$

where γ is the noise parameter, k is the Boltzmann constant, and T is the absolute temperature. Ignoring the effects of MR0-MR3, the output current noise spectral density of the A^2/Hz at z terminal can be obtained as

$$\begin{aligned}\overline{i_{z,out}^2} \approx\ & 8kT\gamma\Bigg\{(g_{mMP1} + g_{mMN13}) + \frac{g_{mMN13}{}^2}{g_{mMN9}{}^2}(g_{mMN9} + g_{mMP0,9}) \\ & + g_{mMN13}^2\Bigg[(g_{mMP5} + g_{mMN10})\Bigg(\frac{1}{g_{mMP0}}\Bigg\|\frac{1}{g_{mMP5}g_{mMN15}r_o} \\ & + \frac{1}{g_{mMN15}}\Bigg)^2\Bigg]\Bigg\} + 8kT\gamma g_{mMP1}{}^2\Bigg\{\Bigg[g_{mMP0} + g_{mMN2} \\ & + \frac{g_{mMN2}{}^2}{g_{mMN1}{}^2}(g_{mMN1} + g_{mMP0,9})\Bigg]\Bigg[\Bigg(1 + \frac{g_{mMN7}}{g_{mMN2}}\Bigg)r_o\Bigg\|\frac{1}{g_{mMP0}}\Bigg]^2\Bigg\}\end{aligned} \tag{36}$$

and the output current noise spectral density of the A^2/Hz at x_i and x_{iz} ($i = 1, 2, ...$) terminal can be obtained as

$$\overline{i^2_{xi,xiz,out}} \approx 8kT\gamma\left\{(g_{mMP12}+g_{mMN27})+\frac{g_{mMP12}{}^2}{g_{mMP11}{}^2}(g_{mMP11}+g_{mMN22})+g_{mMN27}{}^2\left[(g_{mMP18}+g_{mMN26})\left(\frac{1}{g_{mMN26}}\Big\|g_{mMP21}r_{oMP18}r_{oMP21}\right)^2\right]+g_{mMP12}{}^2(g_{mMP10}+g_{mMN19}+g_{mMN16})\left[\frac{1}{g_{mMP12}}\Big\|(r_{oMN18}\|g_{mMN17}r_{oMN17}r_{oMN18})\right]^2\right\} \quad (37)$$

With analysis on Equations (35)–(37), it is indicated that the cascaded stage could add noise while providing high output impedances. And a comparatively low $g_{mMN0,9}$ is helpful for reducing the noise at z terminal, which means an increasing overdrive voltage, however, big value of overdrive voltage brings increased DC supply voltages. Thus, the bias condition of transistors MN0 and MN9 should be provided appropriately to deal with the trade-off between noise performance and power consumption. To reduce output noise at x_i and x_{iz} terminal and improve circuit's signal-to-noise ratio, the transconductance of input transistors (such as MN16-MN21) should be maximized, namely, the aspect ratio of input transistors can be increased reasonably as the drain-source current is to be maintained constant.

Figure 13 shows the output noise spectral density at z, x_i, and x_{iz} terminals of this CDCTA. It can be seen that the output noise of z terminal at 10 MHz is 26.2 pA/sqrt (Hz). The output noise of x_i and x_{iz} ($i = 1, 2, ...$) at 10 MHz is all 36.2 pA/sqrt(Hz). It is clear that the output noise at z, x_i, and x_{iz} terminals is even lower above the frequencies of 10 MHz.

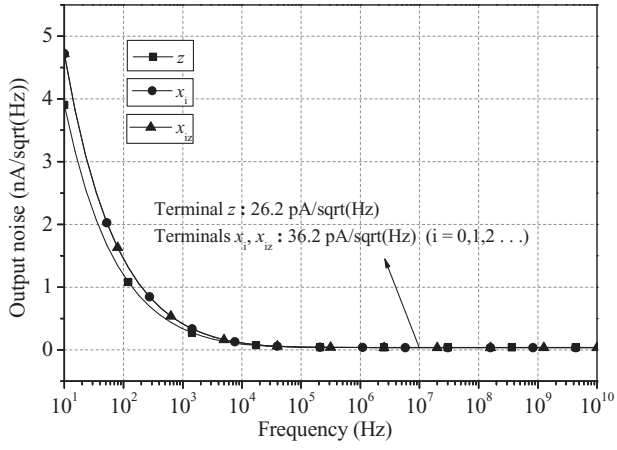

Figure 13: Output noise of terminals of CDCTA

Table 2: Aspect ratios of transistors

MOS transistors	$W(\mu m)/L(\mu m)$
MN0, MN8	8.4/0.3
MN1-MN6, MN9-MN14, MN22-MN29	7.2/0.3
MN7, MN15	40/0.3
MN16-MN21, MN31-MN36, MN46-MN50	12/1
MN30, MN45,MN59,MN63	60/1
MN60-MN62	1.3/1
MP1-MP8, MP10-MP45	34/0.3
MP0, MP9	7.2/0.3
MP46	10.5/1
MP47	81.5/1
MP48	6.3/1
MN49-MN50	52.3/1
MR0-MR1	0.8/0.5
MR2-MR3	18/0.5
MR4-MR5, MR8-MR9, MR12-MR13	0.5/0.9
MR6-MR7, MR10-MR11, MR14-MR15	23/0.5

5. THE DESIGN EXAMPLE AND SIMULATION RESULTS

To verify the performances of the proposed CDCTA, a CM MF filter in Figure 10(a) adopting the proposed circuit is simulated in Cadence Spectre using the BSIM3v3.3 model for a 1.8-V thin-gate MOSFET process using the *GlobalFoundries'0.18* μ*m* technology. The aspect ratios of MOS transistors are listed in Table. 2. The supply voltages are $+V_{DD} = -V_{SS} = 0.8$ V.

Normalized transfer function is

$$H(s) = \frac{1}{s^4 + 2.61313s^3 + 3.4142s^2 + 2.61313s + 1} \quad (38)$$

From Equations (15), (16), and (38), we can conclude $\tau_1 = 0.382683$, $\tau_2 = 1.08239$, $\tau_3 = 1.57716$, and $\tau_4 = 1.53073$. Assume that the CDCTA in Figure 2 is designed with the transconductance values of $g_m = g_{m1} = g_{m2} = g_{m3} = g_{m4}$, and the filter's cut-off frequency f_c is desired, the values of the capacitances can be calculated after denormalization as follows:

$$C_i = \frac{\tau_i \cdot g_m}{2\pi \cdot f_c} (1 \le i \le 4) \quad (39)$$

where equal transconductance of 400 μS is obtained by setting $V_C = V_{C1} = V_{C2} = V_{C3} = V_{C4} = 0.47$ V. Hence, for the −3dB cut-off frequency of filter is 10 MHz, we can get the capacitances $C_1 = 2.436$ pF, $C_2 = 6.89$ pF, $C_3 = 10.04$ pF, and $C_4 = 9.744$ pF. The simulation result of the frequency response of low pass filter is shown in Figure 14, and the symbol "♦" indicates a cut-off frequency f_c of 10 MHz.

It is of great importance that, according to Equation (39), when the capacitances have been set, the −3dB cut-off frequency of low pass filter is proportional to the

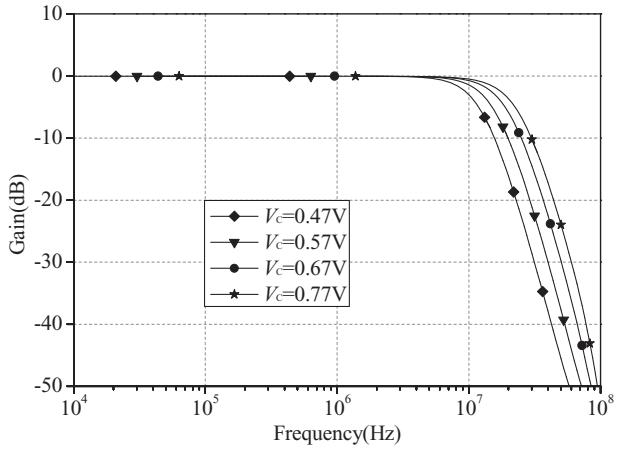

Figure 14: Frequency response of low pass filter for the different V_C

value of the transconductance. As being depicted in Section 2, the value of the transconductance is also proportional to the bias voltage V_C. It is possible that the cut-off frequency can be linearly adjusted by varying V_C while maintaining the capacitance values constant.

As the capacitances are invariable, the g_m values are respectively obtained as 400, 605, 810, and 1016 μS by tuning V_C of 0.47, 0.57, 0.67, and 0.77 V. The cut-off frequencies of the low pass filter can be respectively obtained as 10, 12.92, 15.85, and 18.78 MHz. Figure 14 shows the frequency response of low pass filter for the different V_C. Figure 15 shows the relationship between cut-off frequency f_c of the low pass filter and V_C, the increase of V_C approximately proportionally increases the bandwidth, which is the same as the expected characteristic.

To verify the effects of CDCTA non-idealities, we maintain $V_C = 0.47$ V, then the cut-off frequencies of the

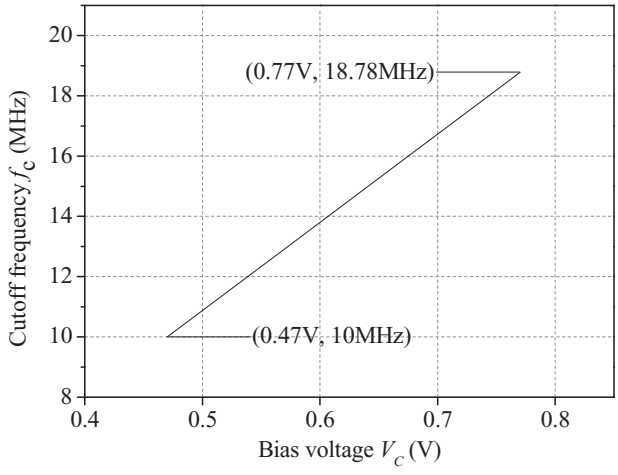

Figure 15: The relationship between cut-off frequency f_c of the low pass filter and V_C

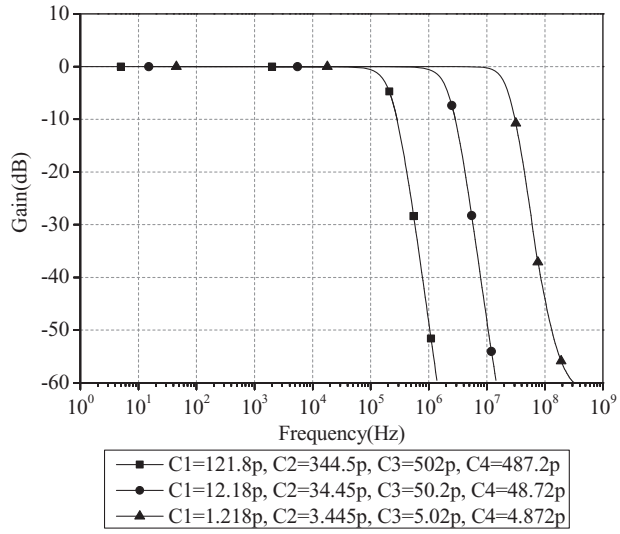

Figure 16: The effects of non-ideal CDCTA to the proposed filter

filter are respectively obtained as 200 KHz, 2 MHz, and 20 MHz by changing the capacitors C_i (i = 1–4). Figure 16 shows the effects of CDCTA non-idealities to the proposed filter, it has a good agreement with theoretical analysis when cut-off frequency is less than 20 MHz. When cut-off frequency is larger than 20 MHz, the impact of parasitic capacitors C_x becomes non-negligible, and non-idealities of the CDCTA need to be considered.

Figure 17 shows the maximum input and output waveform of the proposed filter with a 2 μA, 20 MHz maximum input square signal. The time-domain response of the filter indicates that the switching delay time of the CDCTA is approximately 6 ns and the ripple of the maximum output waveform is small. For testing the large signal behaviour of the proposed filter, total harmonic distortion (THD) versus input current amplitude are shown in Figure 18. It is found that the circuit's THD is not more than 2.9% when current amplitude is less than 50 μA. It is also found that power consumption of the fourth-order filter is only 3.54 mW.

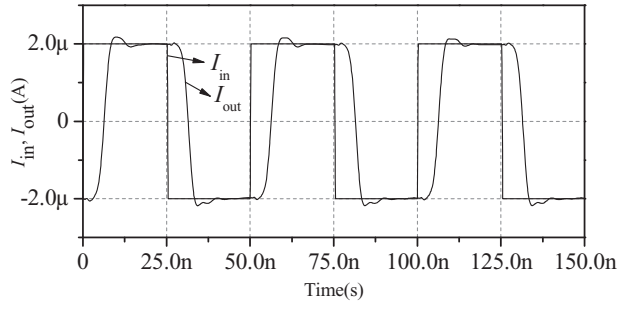

Figure 17: The maximum input and output waveform of the proposed filter

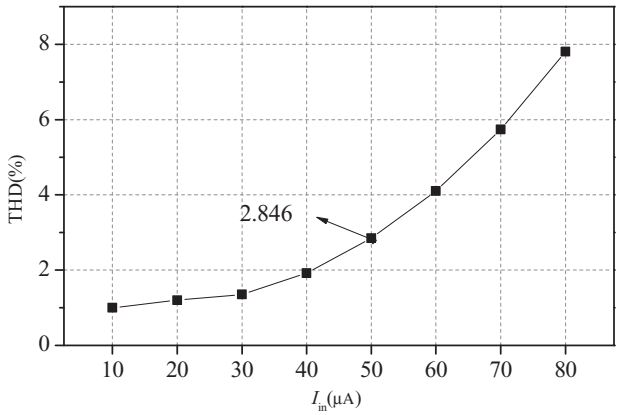

Figure 18: Tested THD versus input current amplitude

The main performances of the proposed MF filter are listed in Table 3, where comparisons with previous work are also provided. From Table 3, the proposed filters adopting only a single active device and *n* grounded capacitors meet the requirement of no active and passive element matching conditions, and have linear-tunable feature and a wide bandwidth with low supply voltage.

6. CONCLUSION

Based on a new CDCTA, a systematic design approach to realize CM MF low pass filters is presented. The proposed CDCTA has linear-tunable feature and wide frequency-bandwidth with low supply voltage (±0.8 V). It simplifies the design of the CM high-order filter considerably. Systematic design generation and synthesis of MF filter structures have been presented. The proposed MF filters enjoy the following advantages. (1) The produced *n*th-order filters adopting only an active component (a CDCTA) and passive elements (*n* grounded capacitors) meet the requirement of no active and passive element matching conditions, it is very appropriate for integrated circuits fabrication. (2) By altering the parameters of the designed matrix, multiple structures of high-order CM all-pole low pass filters can be synthesized without changing internal circuit. (3) It is convenient to linearly tune the filter's frequency by adjusting bias voltage. (4) When the cut-off frequency is less than 20 MHz, the filters are not affected by non-ideal characteristic of CDCTA.

Table 3: The comparison between the proposed high-order filter and previous works

References	[15]	[16]	[11]	This work
Circuit mode	Voltage	Current	Current	Current
Active device	OTA	CFBCCII	OTA	CDCTA
Number of active elements	*n*	*n*	*n*	1
Number of capacitors	*n*	2*n*	*n*	*n*
Supply voltage	NA	±1.5 V	±5 V	±0.8 V
Linear-tunable feature	No	No	No	Yes
Cut-off frequency of filter example (order of the filter)	1 MHz (fourth-order)	10 MHz (fourth-order)	464 KHz (third-order)	20 MHz (fourth-order)

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DISCLOSURE STATEMENT

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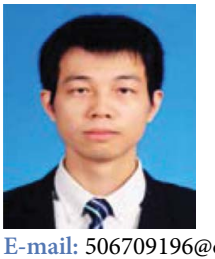

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