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A Multiple-Feedback UWB LNA with Low Noise and Improved Linearity

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ABSTRACT
A 3.1–10.6 GHz CMOS low-noise improved-linearity amplifier (LNA) for ultra-wideband (UWB) applications is presented in this paper. This UWB LNA is designed with multiple-feedback networks and noise/distortion cancellation technique. For better bandwidth extension and less chip-size occupation, a transformer is combined with a shunt feedback resistor to construct the novel multiple-feedback networks. Simultaneously, a modified noise/distortion cancellation technique is adopted in the input stage, to reduce the noise figure (NF) and nonlinear distortion. Simulation results illustrate that this proposed LNA achieves a maximum gain of 14.2 dB with 7.2 mW power dissipation under 1.2 V supply voltage, while having an IIP3 of 4.2 dBm and a minimal NF of 2.5 dB. The chip size is only 0.72 mm × 0.72 mm including the testing pads (core area is 0.57 mm × 0.57 mm).

KEYWORDS
CMOS; Linearization; LNA; Multiple-feedback; Noise-cancellation; UWB

1. INTRODUCTION

As the ultra-wideband (UWB) wireless communication system possesses merits of robustness, flexibility, and low cost for rapid and short-distance data transmission [1,2], it has attracted more and more attention both in academia and industry [3,4]. The low-noise improved-linearity amplifier (LNA) is a significant component in the UWB receiver chain and it vitally influences the entire UWB wireless system [5]. Thus, it is important that the designed LNA can supply sufficient gain and good linearity with minimal noise figure (NF). Compared with traditional single frequency or narrow band LNA, the UWB spectrum ranges from 3.1 to 10.6 GHz. It is a big challenge for UWB LNA to provide good input impedance matching over broad bandwidth about 7.5 GHz without compromising other performances [6–8].

The works reported in [9–11] have realized LNAs with acceptable input matching over 3.1–10.6 GHz, but their NF or linearity is not ideal. Parvizi [12] proposed an LNA with ultra-low power dissipation of 0.25 mW, while its linearity and bandwidth are limited. A 0.8–2.1 GHz broadband LNA with an extremely high linearity of 16 dBm is presented in [13], but it also suffers the bandwidth extension issues. The works reported in [14] and [15] will be listed in comparison table later.

The previous work in [16] adopted multiple-feedback networks to accomplish 3.4–10.1 GHz LNA with 2.33 mW power dissipation at 0.8 V supply voltage based on a forward body bias technique, but the reported LNA's low noise will reduce maximum gain, and the LNA can only provide a limited linearity of −14.36 dBm due to the fact that in its input stage there exists largely nonlinear distortion. Thus, this paper presents a new UWB LNA, which adopts the multiple-feedback networks to cope with broadband input impedance matching problem. Besides, an improved noise-cancelling technique, inspired by [17], is proposed in this LNA in order to achieve desirable linearity and reduced NF while the other performances remain as in the same range of the previous LNA [16].

2. CIRCUIT DESIGN METHODOLOGY

2.1 The Frequency Response Improvement

Generally, the bandwidth of LNA will be constrained by the interstage parasitic reactance when it is cascaded to the next stage. Taking the circuit in Figure 1(a) for an instance, the parasitic capacitance C_{GS} reduces the circuit performances as it bypasses with load resistor R_L, which limits the bandwidth at frequency of $1/(R_L C_{GS})$. To alleviate the influence from C_{GS}, a practical option, illustrated in Figure 1(b), is adopting a series inductor L across R_L and C_{GS}. This creates series peaking in the frequency response and resonates out the parasitic capacitance. With creation of the RLC resonant circuit by L, R_L, and C_{GS}, the $|V_{out}/I_{in}|$, which represents the frequency response, can be derived as follows:

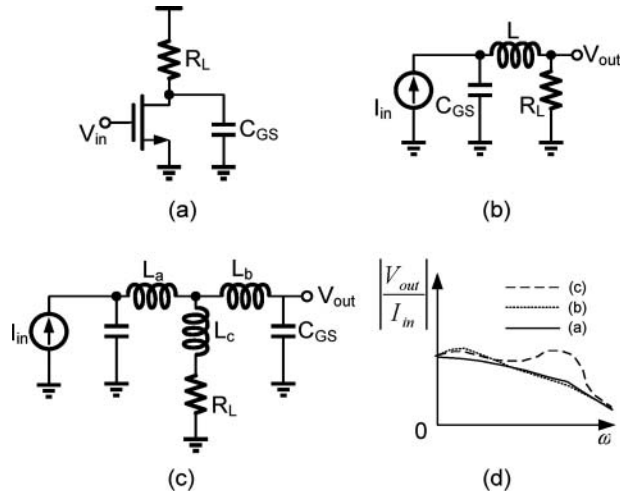

Figure 1: Frequency response performance of different circuits

$$|V_{\text{out}}/I_{\text{in}}| = R/(sLC+sRC+1) \tag{1}$$

To further enhance the frequency response, a series–shunt–series circuit is constructed in Figure 1(c), which includes triple inductors (L_a–$\underline{Lc}$) and can represent a better frequency response. Comparisons of the frequency responses between the three circuits mentioned above are charted in Figure 1(d).

2.2 Linearization and Noise-Cancellation

To operate the LNA in good linearity and low noise, a distortion/noise cancellation technique is utilized in the first stage, which is displayed in Figure 2. The first stage consists of an input impedance matching part (M_{n1}, M_{p1} and R_F) and a noise-cancelling part (M_{n2}, M_{p2} and M_{n3}). For low-power dissipation and desirable wideband input matching, M_{n1} and M_{p1} form a complementary amplifier with resistive shunt feedback R_F. Noise signals generated from these two transistors will be cancelled by the noise-cancelling part.

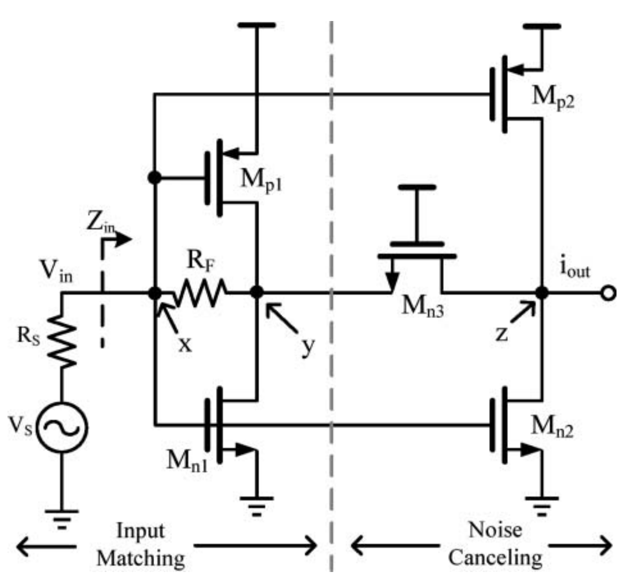

Figure 2: The first stage of LNA

At low frequency, the input impedance will be matched if the following condition is satisfied

$$R_S = Z_{\text{in}} = \frac{1 + g_{mn3}R_F}{g_{mn1} + g_{mp1} + g_{mn3}} \tag{2}$$

where R_S, R_F, Z_{in} are the source resistor, feedback resistor, and input resistance. And g_{mn3}, g_{mp1}, g_{mn1} are the transconductance of transistors M_{n3}, $M_{p1,}$ and M_{n1}, respectively. The noise cancelling technique is working as follows, assuming that the noise voltage at node y is positive and it is subsequently converted into noise current by M_{n3}. At the same time, the noise voltage at node x will be converted into noise current by M_{p2} and M_{n2}. At node z, if these two noise currents from node x and node y are equal, the noise contributed by M_{n1} and M_{p1} will be fully cancelled in output current i_{out}. Then we get the cancellation condition

$$\left(g_{mn2} + g_{mp2}\right)R_S = g_{mn3}(R_S + R_F) \tag{3}$$

where g_{mn2} and g_{mp2} are the transconductance of transistors M_{n2} and M_{p2}. Contrarily, the RF signals flowing through these two paths are converted into RF currents and will be added up with accumulation as they have same polarity. As the noise from M_{n1} and M_{p1} is cancelled, the noise of the first stage will be contributed by R_F, M_{n2}, $M_{n3,}$ and M_{p2}. When the input impedance is matched, the noise output currents of these four devices can be expressed as follows:

$$\overline{|i_{\text{nout}}|^2_{R_F}} = \frac{\left(1/R_S + g_{mn1} + g_{mp1} + g_{mn2}R_F\right)^2 4kT/R_F}{\left(1/R_S + 1/R_F + \left(g_{mn1} + g_{mp1} + 1/R_S\right)/g_{mn3}R_F\right)^2} \tag{4}$$

$$\overline{|i_{\text{nout}}|^2_{M_{n2}}} = 4kT\gamma g_{mn2} \tag{5}$$

$$\overline{|i_{\text{nout}}|^2_{M_{p2}}} = 4kT\gamma g_{mp2} \tag{6}$$

$$\overline{|i_{\text{nout}}|^2_{M_{n3}}} = \frac{4kT\gamma}{1 + g_{mn3}Z_L} \tag{7}$$

where

$$Z_L = \frac{R_S + R_F}{1 + (g_{mn1} + g_{mp1}) R_S} \tag{8}$$

the parameter γ is the noise coefficient in (5)–(7). Hence, the overall NF will be

$$NF = 1 + \frac{\overline{|i_{nout}|^2_{R_F}} + \overline{|i_{nout}|^2_{M_{n2}}} + \overline{|i_{nout}|^2_{M_{p2}}} + \overline{|i_{nout}|^2_{M_{n3}}}}{\overline{|i_{nout}|^2_{R_S}}} \tag{9}$$

where

$$\overline{|i_{nout}|^2_{R_S}} = \frac{4kT}{R_S}(R_S||Z_{in})^2 \left(\frac{2g_{mn2}R_F}{R_S + R_F}\right)^2. \tag{10}$$

With analysis on (9), it is indicated that the M_{n2}, $M_{n3,}$ and R_F primarily contribute to the noise. For getting lower noise, it should choose relatively larger g_{m2} and R_F, but it will consume more power at M_{n2}. Simultaneously, there is a mutual restriction between g_{mn2}, g_{mn3}, and R_F for satisfying the noise elimination condition. Based on these considerations, the larger R_F is selected here to reduce the noise and enhance the gain of LNA; the relatively smaller g_{mn2} and g_{mn3} are selected to ensure that the noise elimination condition is satisfied [18,19]. A positive feedback configuration of M_{N3} can improve gain and reduce noise. Furthermore, big value of R_F is also beneficial to get high gain as a result of

$$A_V = -2(R_F/R_S). \tag{11}$$

According to the discussions above, the noise of M_{n1} and M_{p1} is cancelled by M_{n2}, $M_{n3,}$ and M_{p2}. Moreover, the nonlinear distortion of M_{n1} and M_{p1} will also be diminished upon the satisfaction of the noise cancellation condition (3).

In Figure 3, the small signal equivalent model of input matching part is shown, to analyze the nonlinear distortion of M_{n1} and M_{p1}. The nonlinear distortion in currents (i_{dsp1} and i_{dsp2}) is generated by M_{n1} and M_{p1}, so V_x and V_y will also be nonlinear. The V_x can be expanded as a Taylor series of V_s

$$V_x = x_1 V_S + (x_2 {V_S}^2 + x_3 {V_S}^3 \cdots) = x_1 V_S + V_{nl} \tag{12}$$

where V_{nl} includes all the unexpected nonlinear terms, and $x_n(n = 1,2,3\ldots)$ are the Taylor coefficients. From Figure 3, the V_y can be given by

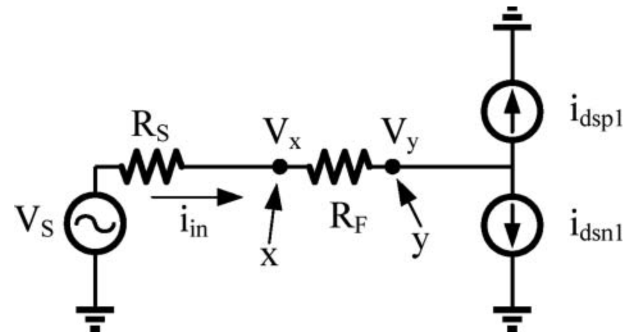

Figure 3: Small signal equivalent model of input matching part

$$V_y R_S = (R_S + R_F)V_x - R_F V_S. \tag{13}$$

The V_x is converted into current (i_{nlx}) by M_{p2} and M_{n2}, the V_y is converted into current (i_{nly}) by M_{n3}. At node z in Figure 2, the output current will be given as follows (the nonliear distortion caused by M_{p2}, $M_{n2,}$ and M_{n3} is neglected here)

$$\begin{aligned} i_{\text{out}} &= i_{\text{nlx}} - i_{\text{nly}} = (g_{mn2} + {}^{mn2} g_{mp2})V_x - g_{mn3}V_y \\ &= \frac{R_F}{R_S} g_{mn3} V_S + \left((g_{mn2} + g_{mp2}) - g_{mn3}\frac{R_S + R_F}{R_S} \right)(x_1 V_S + V_{nl}). \end{aligned} \tag{14}$$

Once (3) is satisfied, the second term of (14) will be zero, so does V_{nl}. This indicates that the nonlinear distortion caused by M_{n1} and M_{p1} is cancelled [20]. Further analysis in detail is addressed in [21]. Then, the linearity of the LNA is dominated by M_{n2} and M_{n3}. To reduce the nonlinear distortion caused by M_{n2} and M_{n3}, the transistor M_{p2} is configured as an auxiliary transistor. At node z, the nonlinear drain currents caused by M_{n2}, $M_{n3,}$ and M_{p2} are i_{n2}, $i_{n3,}$ and i_{p2}, respectively. According to Kirchhoff's Circuit Law (KCL), the output current yields

$$i_{\text{out}} = i_{n2} + i_{n3} - i_{p2}. \tag{15}$$

The drain currents can be expanded in Taylor series

$$i_{n2} = a_{n21}V_x + a_{n22}V_x^2 + a_{n23}V_x^3 \tag{16}$$

$$i_{n3} = a_{n31}V_y + a_{n32}V_y^2 + a_{n33}V_y^3 \tag{17}$$

$$i_{p2} = a_{p21}V_x + a_{p22}V_x^2 + a_{p23}V_x^3 \tag{18}$$

where parameter a_{ij} is the jth-order coefficient of M_{n2}, $M_{n3,}$ and M_{p2} ($i = n2, n3, p2$ and $j = 1, 2, 3$). According to basic circuit theory, the relationship between V_y and V_x is

$$V_y(1 + g_{mn3}R_F) = V_x(1 - g_{mn1}R_F - g_{mp1}R_F) \tag{19}$$

$$V_y/V_x = b\,. \tag{20}$$

With (16)–(20) being substituted into (15), the output current can be expressed by

$$i_{\text{out}} = \left(a_{n21} - ba_{n31} + a_{p21}\right)V_x + \left(a_{n22} + b^2a_{n32} - a_{p22}\right)V_x^2 + \left(a_{n23} - b^3a_{n33} + a_{p23}\right)V_x^3\,. \tag{21}$$

It can be disclosed in (21) that M_{n2} and M_{n3} have the same gate-source voltage, because the nonlinear coefficients are aligned towards the gate-source voltage. Furthermore, both the second-order coefficient $a_{n22} + b^2 a_{n32} - a_{p22}$ and third-order coefficient $a_{n23} - b^3a_{n33} + a_{p23}$ are expected to be minimal. Unfortunately, due to their different amplitude, they cannot be diminished at the same time. Thus, our option here is to eliminate the third-order item with impaired second-order item.

2.3 The Proposed LNA

Based on the frequency response improvement analyzed in Section 2.1 and the distortion/noise cancellation technique considered in Section 2.2, the circuit topology of the proposed LNA with two gain stages is displayed in Figure 4. The first input stage of this LNA utilizes multiple-feedback networks with a distortion/noise cancellation configuration, to accomplish bandwidth extension and reduce NF while possessing a good linearity. Meanwhile, the output stage is buffered and is gain-improved by a common-source amplifier with inductive peaking technique.

For low-voltage and low-power dissipation, the first stage transistor M_{n3} reuses the bleeding current from transistor M_{n4} of the second stage. Furthermore, as discussed in Section 2.1, triple series–shunt–series inductors represent better frequency response and are equivalent to a transformer. The transformer T_f consisting of inductors L_1 and L_2 is adopted, and k is the magnetic coupling coefficient between L_1 and L_2. It not only increases the frequency response of the circuit, but also can effectively save the area of chip. Resistor R_F across gate and drain of M_{n1} sends back the AC small signal and produces a resistive shunt feedback second-order band-pass filter. The resistor R_F and transformer T_f construct the multiple-feedback networks. Interstage

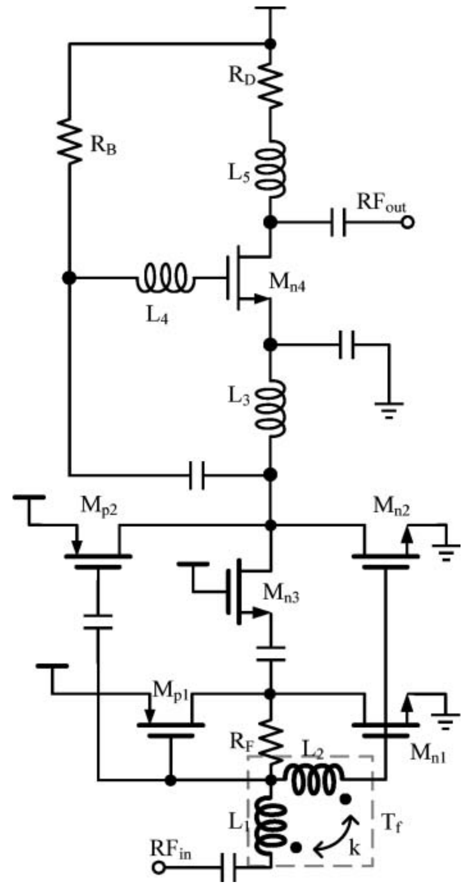

Figure 4: The proposed LNA

matching is completed by L_3 and L_4. L_5 is inserted between M_{n4} and R_D as part of load to improve gain flatness and to eliminate the drain pole parasitic capacitance of M_{n4}.

3. RESULTS AND DISCUSSIONS

The proposed UWB LNA is implemented by Cadence IC Design Tools Spectre RF under standard Charted 0.18 μm RF CMOS technology. All components in this LNA use ideal models in the pre-layout simulation, and use foundry models of Global Foundries in post-layout simulation to better approximate the hardware results.

The simulation results of scattering parameters for this proposed LNA are charted in Figures 5 and 6. The input return loss parameter S11 is an indicator of the input impedance matching performance. Both in the pre-layout and post-layout simulation, the S11 parameters are less than −10 dB from 3.1 to 10.6 GHz. This implies that the multiple-feedback networks adopted in the input stage of this LNA is efficient for bandwidth extension. Moreover, the output return loss parameter S22 is also under −10 dB as well as S11 in the pre-layout

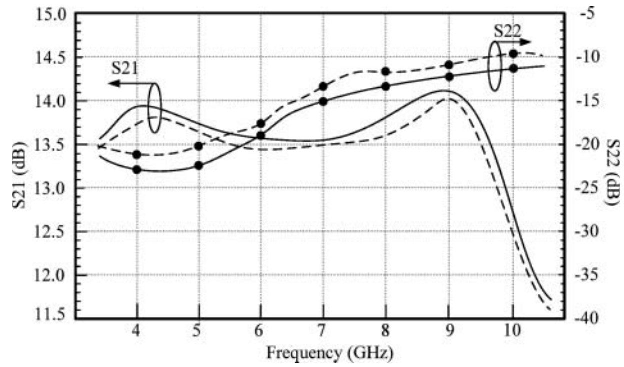

Figure 5: Pre-layout (solid line) and post-layout (dotted line) S21, S22 versus frequency

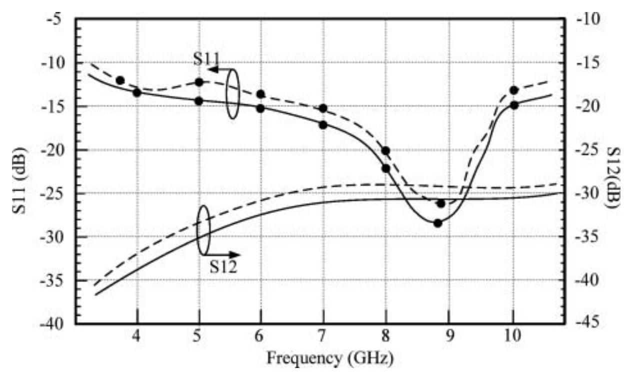

Figure 6: Pre-layout (solid line) and post-layout (dotted line) S11, S12 versus frequency

simulation. In the post-layout simulation, S22 is a little bigger than −10 dB around 10 GHz. This is caused by the process variation. Acceptable S11 and S22 indicate that this LNA has good input and output impedance matching performance over the whole expected bandwidth.

As marked in Figure 6, the reverse isolation parameter S12 is underneath −30 dB in pre-layout simulation, the signal exported in output terminal of the LNA is ideally isolated from the input signal. In other words, the output signal will not be interfered by the imported signal from the input terminal. However, in the post-layout simulation, the S12 is larger than −30 dB from 6.5 to 10.6 GHz. This results from the leakage of input and output signals through the substrate. The gain of the LNA is denoted by S21, which is larger than 11.7 dB from 3.1 to 10.6 GHz and achieves maximum gain of 14.2 dB at 8.9 GHz in the pre-layout simulation. The S21 in the post-layout simulation reduces 0.2 dB over the whole UWB spectrum.

It is evident in Figure 7 that the NF of this LNA is not degraded while the scattering parameters are desirable.

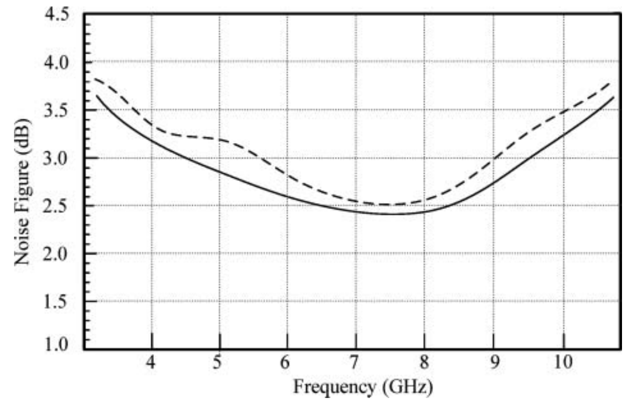

Figure 7: Pre-layout (solid line) and post-layout (dotted line) noise figure versus frequency

This acceptable phenomenon is a benefit from the noise-cancelling technique realized in this LNA. From 3.1 to 10.6 GHz in the post-layout simulation, the NF of this LNA is less than 3.8 dB, and have a minimum value of 2.5 dB around 7.5 GHz.

The input-referred 1 dB compression point (IP1) of this LNA is displayed in Figure 8. The IP1 is −8.1 dBm. Figure 9 shows the IIP3 is 4.2 dBm. These two post-layout simulational results are performed at 5.2 GHz, and they validate the theoretical analysis in Section 2.2. The linearity of the LNA is improved by the modified noise/distortion cancellation technique.

The IIP3 versus frequency is charted in Figure 10, the IIP3 peaks around 4.2 dBm at 5.2 GHz and its minimal value is about 2.5 dBm at 3.1 GHz. This indicates that the IIP3 is acceptable over UWB frequency range. To further test the robustness of this proposed UWB LNA under different conditions, of which S11, NF, S21, and IIP3 for three corners including Corner1 (65 °C, TT), Corner2 (−25 °C, FF) and Corner3 (100 °C, SS) are simulated in Figures 11 and 12, respectively.

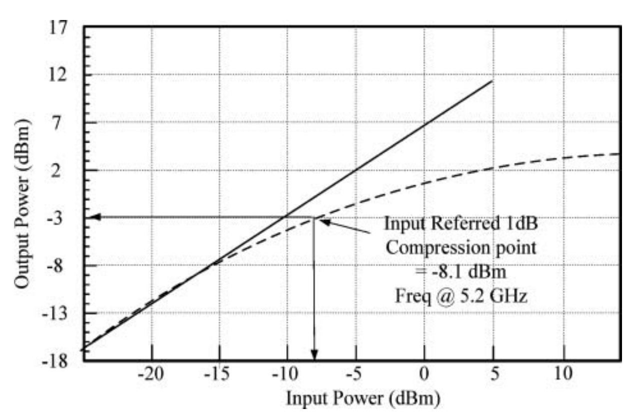

Figure 8: Post-layout 1 dB compression point curve

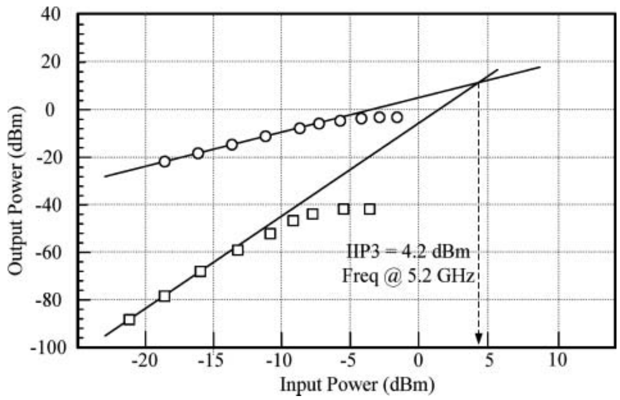

Figure 9: Post-layout IIP3

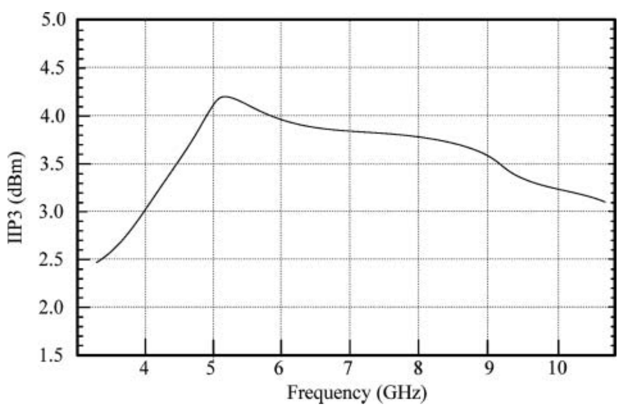

Figure 10: IIP3 versus frequency

Figure 11 shows that the LNA in Corner1 possesses better S11 performance than other two corners. The S11 in Corner3 is less than −10 dB implying this LNA has good input matching. The NF of Corner3 is the highest but still lower than 3.8 dB, which means the noise of the LNA is well restrained. Furthermore, the S21 of all three corners in Figure 12 are larger than 11.5 dB and the IIP3 are bigger than 2.3 dBm, the gain and linearity are good.

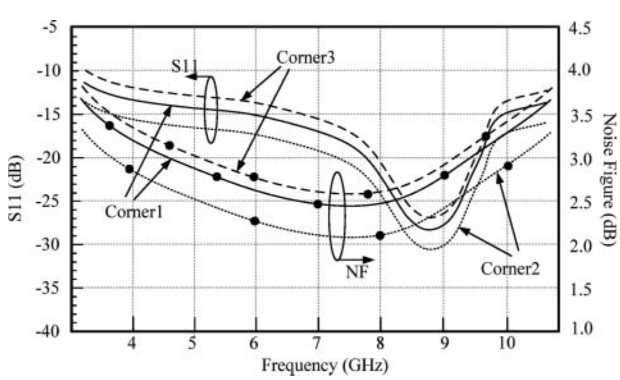

Figure 11: S11 and NF versus frequency for three corners

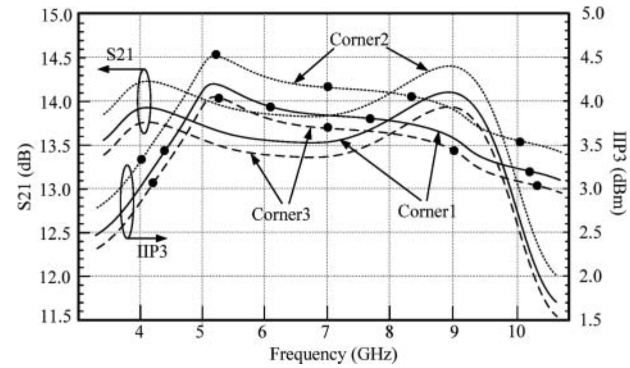

Figure 12: S21 and IIP3 versus frequency for three corners

Figure 13 indicates that an increase in frequency space causes a decrease in IIP3.

The layout of this LNA is shown in Figure 14. It occupies a compact chip area about 0.72 mm × 0.72 mm including the testing pads (core area is 0.57 mm × 0.57 mm). Table 1 summarizes and compares the performances of the proposed LNA with other recently reported relevant works. This LNA achieves a gain of 14.2 dB over 3.1–10.6 GHz with 7.2 mW power consumption. The NF is relatively lower and the linearity is better than all mentioned works, which makes this LNA more competitive. The figure of merit (FOM) in Table 1 is calculated as follows:

$$\mathrm{FOM} = \frac{IIP3[mW] \times \mathrm{Gain}[abs] \times BW[GHz]}{\mathrm{Power}[mW] \times (NF - 1)}. \tag{22}$$

According to (22), this proposed UWB LNA has achieved a relatively good FOM value of 18.05 compared with the other works.

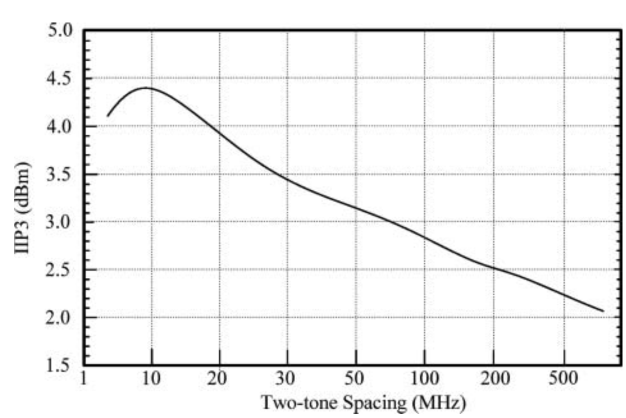

Figure 13: IIP3 versus two-tone spacing

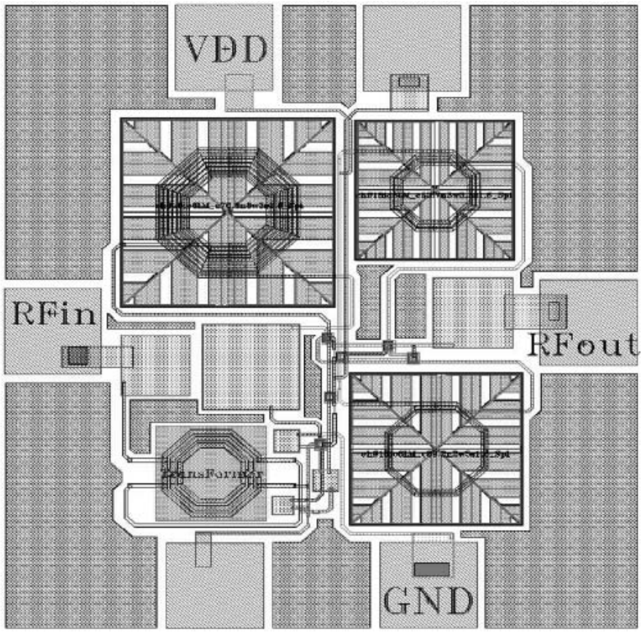

Figure 14: Layout of the proposed LNA

Table 1: **Summary and Comparison of broadband LNA**

Ref.	Supply (V)	Power (mW)	NF_{min}(dB)	$Gain_{max}$ (dB)	S11 (dB)	IIP3 (dBm)	BW(GHz)	Tech. (μm)	Area (mm^2)	FOM
[6][a]	1.8	15.2	2.9	12.6	<-10	−4.6	3.1–10.6	0.18	NG[b]	0.77
[7][a]	0.6	4.33	1.11	20	<-10	−22	3.1–10.6	0.09	NG	0.38
[8][a]	1.5	9	2.2	15.1	<-10.6	−6.0	3.1–10.6	0.18	0.53	1.81
[9]	1.5	13.4	2.5	12.7	<-9	−3	3.1–10.3	0.18	0.68	1.49
[10]	1.2	9	2.5	15.1	<-10	3	3.1–10.6	0.13	0.574	12.15
[11]	1.2	13	4.8	17	<-14	−1.53	3.5–10	0.13	0.35	1.23
[12]	0.5	0.25	4	14	<-9	−10	0.6–4.2	0.13	0.39	4.82
[14]	1.1	2.15	4.58	10.4	<-10.1	−5.4	2.8–10.4	0.18	0.734	1.71
[15]	0.4	0.41	4.5	15	<-10	−2	3.2–10	0.09	NG	32.54
[18]	0.5	0.75	5.5	12.6	<-10	−6	0.1–7	0.09	0.23	4.26
[19]	1	0.4	4.9	12.3	<-9	−9.5	0.1–2.2	0.13	0.0052	1.236
This work[a]	1.2	7.2	2.5	14.2	<-10	4.2	3.1–10.6	0.18	0.32	18.05

[a]Simulational results.
[b]Not given.

4. CONCLUSIONS

This paper presents a 3.1–10.6 GHz broadband low-noise improved linear CMOS LNA for UWB receiver; the proposed circuit utilizes a multiple-feedback network for desirable bandwidth extension and low chip area occupation. By using noise/distortion cancellation techniques in circuit design, the NF is reduced and nonlinear distortion is improved. Compared with the other reported LNAs, this LNA has a comparable maximum gain of 14.2 dB at 1.2 V supply voltage with 7.2 mW, while the NF is well constrained under 3.8 dB and the linearity can reach up to 4.2 dBm. Therefore, this LNA can be applied in many UWB applications, especially in some mobile applications requiring low noise and high linearity.

DISCLOSURE STATEMENT

No potential conflict of interest was reported by the authors.

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