



Emotion model of associative memory possessing variable learning rates with time delay[☆]



Linmao Yang, Chunhua Wang^{*}

College of Computer Science and Electronic Engineering, Hunan University, Changsha 410082, China

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ABSTRACT

Lots of researchers have used memristors to realize the emotion model of associative memory. In previous works, researchers analyzed this associative memory from two perspectives—forgetting and variable learning rate. In the previous emotion model, neutral stimulus(message notification) and unconditioned reflex(good or bad message) were applied simultaneously. But the variable learning rate with time delay is not considered in the emotion model. When the unconditioned reflex lags behind the neutral stimulus, the associative memory can also be formed. This article proposes an emotion model of variable learning rate with time delay. We also consider three kinds of forgetting: only a stimulus of unconditioned reflex applied, only a neutral stimulus applied and neither stimulus of unconditioned reflex nor neutral stimulus applied. In the end, the software PSPICE is used to simulate the whole circuit. This paper provides an option to realize emotional learning based on memristor.

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1. Introduction

The memristor, as a basic circuit element, was predicted by Chua in 1971 [1] for the first time and manufactured by HP Labs in 2008 [2] for the first time. And then, many other kinds of memristors have been proposed [3]. However, the manufacture of memristor is complex. In order to study its characteristics, apart from the physical memristor, some researchers used CMOS circuits to design memristor emulators [4], and others used mathematical models to simulate real objects [5]. Due to its unique nonvolatile storage, non-linearity and nanoscale size, memristor has been widely used in many areas of scientific researches, such as neural network [6–11] and chaotic circuit [12–17].

Artificial neural network (ANN) is the main trend of intelligent computing. Through its unique learning ability, some functions can be achieved, such as image processing [18–20], unsupervised learning [21], supervised learning [22], reinforcement learning [23] and so on. But most of them are realized by software, compared with hardware, the realization of software needs more complex structure and longer processing time. Electronic synapse is the

most important component in the design of ANN circuit. Traditional synapses were formed by MOS transistors, and its structure is complex. Memristor as a nanoscale device is the best candidate for synapse. It reflects the relationship of charge and flux, memristance will be changed according to the current which passes through it or voltage which is applied to it. When the power is cut off (current becomes zero), the memristance remains the same. So memristor can achieve synaptic plasticity well. In the future, memristor is likely to break the limit of von Neumann architecture [24].

In artificial intelligence, emotional models are very important. In the fields of psychology and physiology, one of the emotional models is discrete emotion model [25]. Researchers think that humans have some basic emotions, such as six basic emotions theoretically [26]. The complex emotions are evolved from basic emotions [27]. It is similar to the principle that three primary colors can form any color. For emotion, it can also produce associative memory. When we first hear the message notification, we will not have any emotional fluctuations; but when we check the content of this message and find it is a good message, we will feel happy. If the message notification and a good message appear simultaneously for a while, a connection between message notification and a good mood will be formed. When the message notification appears alone next time, we will feel happy. If we change the good message above into bad message, the corresponding emotion will be sad. This is the emotion of associative memory which has been researched by previous works [28–30]. The details of this model

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^{*} Corresponding.

E-mail address: wch1227164@hnu.edu.cn (C. Wang).

will be introduced in Section 2.2. Wang et al. designed a circuit to simulate the functions of emotional generation and evolution [31]. Paper [30] realized the emotion model of associative memory, but the forgetting and the variable learning rate were not considered. A model of memristor-based associative memory neural network (m-ASNN) for modeling the affections was proposed in [28], but this paper only implemented the associative memory and the processes of forgetting. In [29], the three processes of forgetting and the variable rates of learning were realized in emotion model. Wang et al. designed a multi-associative learning circuit that can produce new complex emotions [32]. In previous works, researchers analyzed this model from two perspectives—forgetting and variable learning rate. But the case with time delay is not considered in the emotion model. In addition when the time delay exists, the learning rate can also be variable, this situation is not considered in previous works.

In associative memory, the first learning needs a period of time. After the first learning, if there is another learning, the learning time will be shorter than before. This is the variable learning rate. It is widely researched in previous works [29,33]. When the time delay exists in the emotion model(the time delay will be described in the next paragraph), the learning rate can also be variable, this situation is not considered in previous works.

In this emotion model, the message notification is called neutral stimulation. The good(bad) message can cause emotional fluctuations, this phenomenon is called unconditioned reflex. Neutral stimulation does not produce any emotional fluctuations, only after acquired learning, it can cause emotional changes alone. The unconditioned reflex is innate, it can produce emotional changes without learning. In these articles, neutral stimulation and unconditioned reflex happen at the same time. But when neutral stimulation is earlier than unconditioned reflex, associative memory can be established as well [33]. Paper [33] realized pavlov associative memory with time delay. However, the case with time delay has not been considered in the emotion model so far. In this article, we realize this function. In this case, message notification and good message often do not appear at the same time. We often hear the message notification first and then check if the content of the message is good or bad. For example, when the mobile phone receives a text message, we hear the SMS ringtone of mobile phone first and then check the message content. So, it makes sense to study this emotion model when there is a time delay between neutral stimulation and unconditioned reflex. In this article, this more useful function is considered.

As described above, this article realizes a new function which is the variable learning rate with time delay in an emotion model. The rest sections of the article are structured as follows. Section 2 introduces two memristor models and an emotion model with associative memory. Section 3 introduces the circuit realization of the emotion model in detail. This section includes input neuron, output neuron, synapse, time delay module and rate variation module. Section 4 is the simulation result of the whole circuit with PSPICE. Section 5 is the conclusion part.

2. Model introduction

2.1. Memristor model

As a new circuit component, memristor represents the relationship between charge and flux. Among different kinds of memristor models, the most researched model is TiO2 memristor model from HP laboratory [2], but this model ignores the border effect. To solve this problem, lots of researchers added the window function to make it accord with the physical memristor [34]. In previous works, there were a variety of mathematical memristor models

[35]. Two memristor models are selected in this work, one is HP memristor model with Biolek window function [36], the other is Ag/AgInSbTe/Ta-based model with threshold voltage [37].

The mathematical expression of HP memristor model is as follows.

$$M(t) = R_{ON}x(t) + R_{OFF}(1 - x(t)) \tag{1}$$

$$x(t) = (w(t))/D \in (0, 1) \tag{2}$$

In the equation, $M(t)$ is memristance of memristor, R_{OFF} and R_{ON} are the maximum and minimum memristance respectively. $w(t)$ is the width of the doped region. D is the length of memristor. In order to realize the nonlinear modeling, paper [39] proposed a window function as follows.

$$\frac{dx}{dt} = kF(X)i(t) \tag{3}$$

$$F(x) = 1 - (x - stp(-i))^{2p} \tag{4}$$

where p is a positive integer, $stp(\cdot)$ is the step function, $k = \frac{\mu_v R_{ON}}{D^2}$ is the so-called dopant mobility. This memristor model is used in input neuron. Fig. 1(b) shows the memristance changes over time when the voltage shown in Fig. 1(a) is applied. In this test, we set $R_{ON}=5(\Omega)$, $R_{OFF} = 2.6 \text{ K}(\Omega)$, $R_{init} = 2.5 \text{ K}(\Omega)$, $D = 10(\text{nm})$, $\mu_v = 1.0 \times 10^{-14} \text{ m}^2 \text{ S}^{-1} \Omega^{-1}$, $P = 1$. R_{init} is the initial memristance value of memristor.

Memristor model with threshold voltage is used in three modules—synapse, time delay module and rate change module. These modules will be introduced in detail in the third part. Ag/AgInSbTe/Ta-based model is closer to the physical memristor than other mathematical memristors [37]. If a positive voltage that exceeds the positive threshold is applied to memristor, the memristance will decrease fast at first and decrease slowly at the end. If a negative voltage which is smaller than the negative threshold is applied to memristor, the memristance will increase fast at first and increase slowly at the end. If the voltage is smaller than the threshold, the memristance will not change. The derivative of the state variable $w(t)$ of this model is

$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \frac{R_{ON}}{D} \frac{i_{off}}{i(t)-i_0} f(w(t)), & v(t) > V_{T+} > 0 \\ 0 & V_{T-} \leq v(t) \leq V_{T+} \\ \mu_v \frac{R_{ON}}{D} \frac{i(t)}{i_{on}} f(w(t)) & v(t) < V_{T-} < 0 \end{cases} \tag{5}$$

$$f(w(t)) = 1 - \left(\frac{2w(t)}{D} - 1\right)^{2p} \tag{6}$$

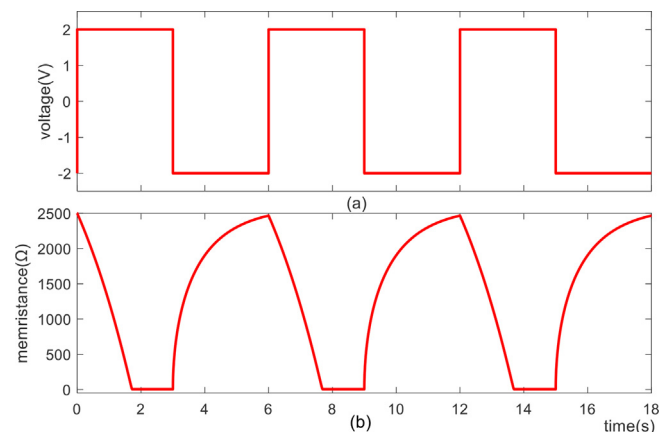


Fig. 1. PSPICE simulation of memristor model with Biolek window function. (a) Input voltage. (b) Changes of memristance.

where i_0 , i_{off} , and i_{on} are constants, V_{T+} and V_{T-} are positive and negative threshold voltages respectively, $f(w(t))$ is the window function. Fig. 2 shows the memristance changes with the applied voltage. In this test, $R_{ON} = 80\Omega$, $R_{OFF} = 3\text{ K}\Omega$, $R_{init} = 2.9\text{ K}\Omega$, $D = 3 \times 10^{-9}\text{ nm}$, $\mu_v = 5.0 \times 10^{-10}\text{ m}^2\text{S}^{-1}\Omega^{-1}$, $P = 10$, $V_{ON} = 1\text{ V}$, $V_{OFF} = -1\text{ V}$, $I_{OFF} = 1.5 \times 10^{-5}$, $I_0 = 1.0 \times 10^{-6}$, $I_{ON} = 0.5$. We can see the threshold voltage and the change rate of memristance obviously.

Fig. 3 shows another unique feature of this model. If amplitudes of voltages are different, textcoloredchanging rates of memristor will be different. A pulse signal is used in this test, the period is 20s, duty cycle is 50%, voltage amplitude is $X(V)$, X is variable. Red line and blue line represent $X = 2\text{ V}$ and $X = 3\text{ V}$ respectively. The result shows, the greater the amplitude of negative voltage is, the faster the increase rate of memristance will become. The greater the positive voltage is, the slower the decrease rate of memristance will become. This feature can be used to realize the variable rate of learning. In this test, we set $R_{ON} = 80\Omega$, $R_{OFF} = 3\text{ K}\Omega$, $R_{init} = 200\Omega$, $D = 3 \times 10^{-9}\text{ nm}$, $\mu_v = 5.0 \times 10^{-9}\text{ m}^2\text{S}^{-1}\Omega^{-1}$, $P = 10$, $V_{ON} = 1\text{ V}$, $V_{OFF} = -1\text{ V}$, $I_{OFF} = 0.5 \times 10^{-5}$, $I_0 = 1.0 \times 10^{-6}$, $I_{ON} = 1$. Biolek window function is used in this test.

2.2. Emotion model

2.2.1. Existing model

In this article, an emotion model with associative memory is selected. In previous works, researchers only realized the functions of basic associative memory which are three forgetting processes and variable rate of learning [30,28,29]. They did not consider the variable learning rate with time delay. In this article, variable learning rate with time delay is considered.

Fig. 4 shows the emotion model. GM, MN and BM are three input neurons, represent good message, message notification and bad message respectively. HN and SN are two output neurons, represent happy neuron and sad neuron respectively. In this emotion model, the message notification is called neutral stimulation. The good(bad) message can cause emotional fluctuations, this phenomenon is called unconditioned reflex. Good message can make people feel happy, this is the innate ability. That is to say, the HN neuron will output a signal as long as GM neuron fires. Hence, we use resistors to represent this inherent synaptic weight. However, the relationship between MN and HN is conditioned reflex. Message notification can not make people feel happy at first. Only

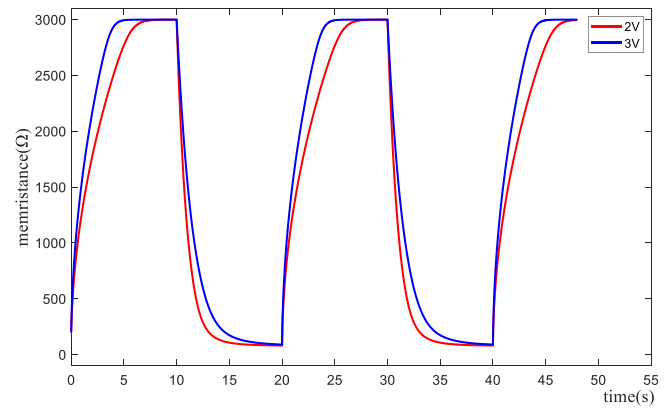


Fig. 3. Memristance changes at different voltage.

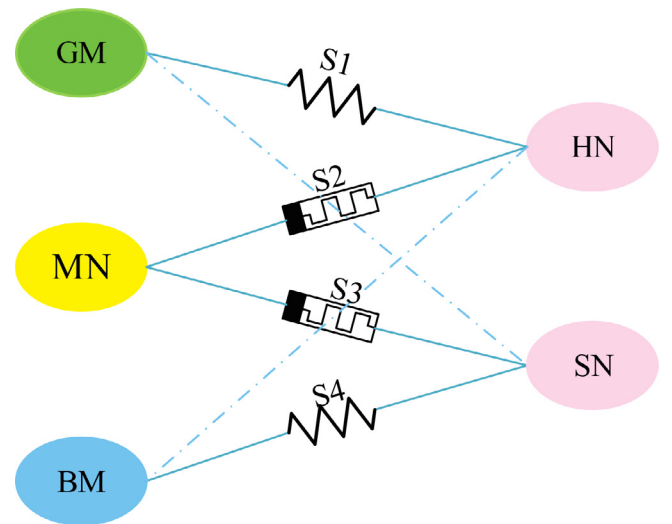


Fig. 4. Emotion model.

through learning can establish the relation between MN and HN. In other word, synaptic weight between these two neurons can be adjusted, therefore, this model uses memristor to realize this function. Obviously, good message can not make people feel sad. So, the dotted line means that the synapse weight between GM and SN is almost zero. To the bad message, the analysis method is the same as good message.

2.2.2. Proposed emotion model of variable learning rate with time delay

In previous works, good message and message notification were applied simultaneously [28,29]. But when neutral stimulation (MN) is earlier than unconditioned reflex, associative memory can be established as well. This process is called time delay learning.

In our daily life, we hear the SMS ringtone firstly and then read the text. In this process, SMS ringtone and read message content have a chronological order. A good message content can make us feel happy. But an SMS ringtone will not produce any emotional fluctuations. Through the delay learning method, we can have a new explanation of this emotion model. In this model, GM, MN and BM are equivalent to good message content, SMS ringtone and bad message content respectively. Table 1. shows this simple associative learning. Because the future learning is the same as the second learning, we only explain the second learning.

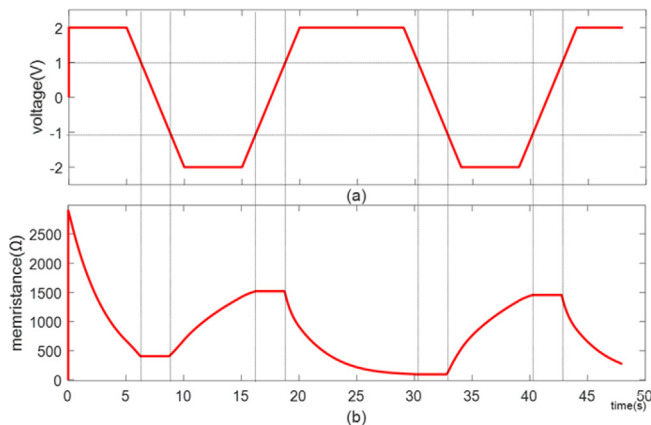


Fig. 2. PSPICE simulation of Ag/AgInSbTe/Ta-based memristor model (a) Input voltage. (b) Changes of memristance.

Table 1
Processes of associative learning

step	input	result
At the beginning	①Only good message (bad message)	Happy(sad)
	②Only message notification	No emotion
First learning	①The message notification is applied firstly	No emotion
	②After a while (time delay), a good message (bad message) is applied	Happy(sad)
	③Next time, when only message notification is applied.	Happy(sad)
forgetting I	①Only good message (bad message) is continued for a period of time	Happy(sad)
	②Next time, when only message notification is applied.	No emotion
forgetting II	①Only message notification is continued for a period of time	No emotion
	Next time, when only message notification is applied	No emotion
forgetting III	①Neither good message (bad message) nor message notification is continued for a period of time	No emotion
	②Next time, when only message notification is applied	No emotion
Second learning	①The message notification is applied firstly	No emotion
	②After a while (time delay), a good message (bad message) is applied	Happy(sad)
	③Next time, when only message notification is applied.	Happy(sad). But the learning time is shorter than before. (variable learning rate)

3. Circuit design

The whole circuit contains five modules. The first module is the input neuron, which realizes production of the pulse signal. The second module is the output neuron, which outputs the final signal. The third module is the synapse, which realizes the connection between neurons. The fourth module is the time delay module, which realizes the learning with time delay. The last module is the rate variation module, which makes learning rate variable.

3.1. Input neuron

If the received signal exceeds the threshold, neurons will output a pulse signal. This is the function of neurons. In previous works, most researchers used the leaky integrate-and-fire neuron model as input neuron [32,38]. Some used Operational Amplifier [39] and 555 timer [40]. Inspired by the circuit designed in [41]. In this article, we use memristor instead of capacitor to design input neuron. Fig. 5 shows the circuit structure.

V_{in} and V_{out} are input and output voltages respectively. VCC is the DC voltage source of 2 V. M1, M4 and M6 are NMOS transistors, and M2, M3 and M5 are PMOS transistors. M1, R1 and M2 realize the function of switch. Threshold voltage of M1 represents the threshold of input neuron. If the input voltage exceeds threshold, potential of M1 drain electrode will be 0 V, M2 works at on-state. Otherwise, resistance of M2 is infinite, the circuit behind will not work. State of M3, M4, M5 and M6 are controlled by the output of D flip-flop. If the output of D flip-flop is 0, M3 and M6 work at on-state, M4 and M5 work at off-state. The circuit marked by red arrow will work. This situation will lead to a decrease of memristance, and then, cause the potential of point A to rise. If the output of D flip-flop is 1, M3 and M6 work at off-state, M4 and M5 work at on-state. The circuit marked by blue arrow will work. This situation will lead to an increase of memristance, and then, cause the potential of point A to rise. Therefore, both these two situations cause the voltage of point A to rise. Component U1 is a Schmitt trigger, if the input voltage exceeds the positive threshold, it will produce a rising edge of signal. If the input voltage is smaller than negative threshold, it will produce a falling edge signal. D flip-flop is to compose a binary adder, every rising edge of signal will cause the output signal to alternate between 0 and 1.

The initial output state of D flip-flop is 0, the initial memristance of M is a large value. So, a small voltage which is smaller than negative threshold of U1 is gotten at point A. As the memristance

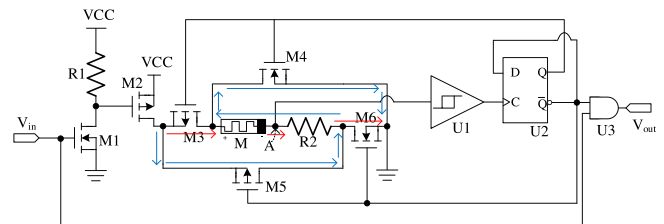


Fig. 5. Circuit of input neuron.

decreases, voltage of point A rises. When the voltage exceeds the positive threshold, U1 produces a rising edge signal to cause the output of D flip-flop to alternate. At this time, memristance of M is small, circuit marked by blue arrow works, voltage of point A is smaller than negative threshold of U1, U1 will produce a falling edge of signal. As the memristance increases, voltage of point A rises. When the voltage exceeds the positive threshold, the output of D flip-flop alternates. So, again and again, the output of D flip-flop will produce a pulse signal. When there is no input signal, output of D flip-flop may be 1, so, at the end of circuit, we add an AND gate. The properties of pulse signal can be adjusted by changing the values of VCC, memristor and R.

Fig. 6 shows the input signal and output signal of input neuron. In this module, HP memristor model with Biolek window function is selected. We set $VCC = 2\text{ V}$, $R_1 = 1\text{ k}(\Omega)$, $R_{ON} = 10(\Omega)$, $R_{OFF} = 2.6\text{ K}(\Omega)$, $R_{init} = 2.5\text{ K}(\Omega)$, $D = 10(\text{nm})$, $\mu_v = 5.0 \times 10^{-14}\text{ m}^2\text{ S}^{-1}\Omega^{-1}$, $P = 1$.

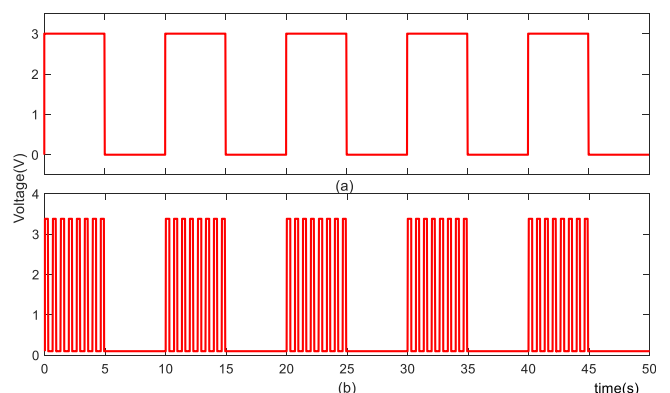


Fig. 6. Function of input neuron (a) input signal (b) output signal.

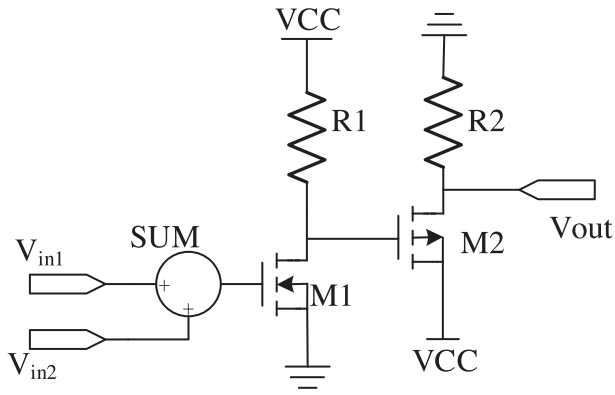


Fig. 7. Circuit of output neuron.

3.2. Output neuron

The function of output neuron is to produce pulse signals when the input signals exceed the threshold. Because the input signal is pulse signal, a simple comparator can be used to design output neuron.

The circuit structure is shown in Fig. 7. VCC is a DC voltage source of 3 V, resistance of R1 and R2 is 1 k(Ω). Turn-on voltage of M1 represents threshold of output neuron. Component SUM is an analog adder, sum all outputs from the synapses connected with it. If signal exceeds threshold, it will produce a voltage of 3 V. Due to input signal is pulse signal, the output signal is pulse signal too.

3.3. Synapse

The function of synapse is to receive the signals from presynaptic neurons connected with it, and then transmits signals to postsynaptic neurons. In order to realize this function, principle of voltage division in circuit theory is used in this article. Fig. 8 shows

the structure of the simple synapses of unconditioned reflex and conditioned reflex. Fig. 8(a) shows the synapse of unconditioned reflex. Due to unconditioned reflex is innate, do not need to learn. This synapse can output a signal which exceeds the threshold of postsynaptic neuron as long as there is a signal from presynaptic neurons. Therefore, two resistors are selected to constitute the synapse. Fig. 8(b) shows the synapse of conditioned reflex. The first component is an analog adder, which receives the signal from three modules. M is a memristor. ABM is a component called as LIMIT in software PSPICE to restrict the negative signal to transmit to postsynaptic neuron. The initial memristance of M is set very large, because the conditioned reflex can't produce output signal at first, only after learning the postsynaptic neuron can react to signals from synapse. More details on how it works will be explained in part 3.5.

3.4. Time delay module and rate variation module

In previous works, the message notification and good(bad) message are applied simultaneously. But when neutral stimulation is earlier than unconditioned reflex, associative memory can be established as well. Of course, delay time is limited. If time interval is too long, associative memory can not be taken shape. Therefore, the function of time delay module is to store the message notification signal for a while. If the good message comes, good message and storage message will change the synapse weight together. If there is no message notification, the storage signal will disappear gradually. Hence a circuit of signal storage is designed as Fig. 9. In this circuit, VCC1 = 5 V, VCC2 = 3 V. Resistance of all resistors is 1 k(Ω) except R3 = 600(Ω). The input port is connected to the output of message notification neuron. If there is an input signal, M4 and M5 work at on-state, the circuit marked by blue arrow will work. Memristance of M will decrease. Otherwise, Memristance of M will increase. If the memristance decreases to a very small value, and then we remove the input signal, the circuit marked by red

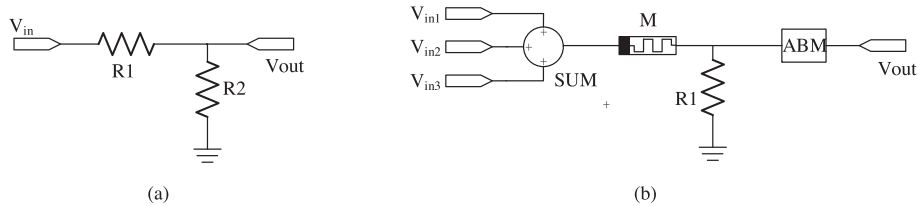


Fig. 8. Circuit structure of synapse (a) Synapse of unconditioned reflex. (b) Synapse of conditioned reflex.

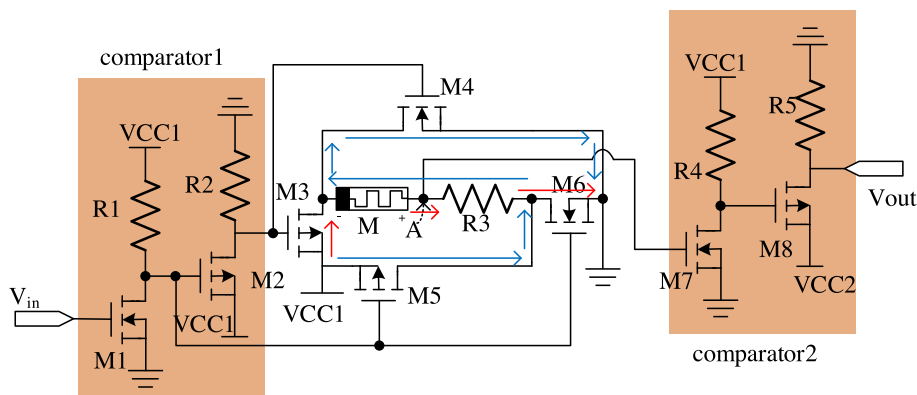


Fig. 9. Circuit of signal storage.

arrow will work. Voltage of point A will be very large, so comparator2 has a high-level output voltage. But the circuit marked by red arrow causes the voltage of point A to decrease gradually. That is to say, storage time is not infinite. The whole circuit of time delay module is shown in Fig. 10(a). Only when good messages(bad messages) but not message notifications are received, the time delay module will output signals. Therefore, NOT gate and AND gate are used to limit the output signal. V_{in1} , V_{in2} and V_{in3} represent input signal. V_{in1} is the output signal of message notification neuron shown in Fig. 5. V_{in2} and V_{in3} are input signal of message notification neuron and good message neuron respectively. In this module, parameters of Ag/AgInSbTe/Ta-based model is as follows: $R_{ON} = 80\Omega$, $R_{OFF} = 3\text{ K}\Omega$, $R_{init} = 2.9\text{ K}\Omega$, $D = 3 \times 10^{-9}\text{nm}$, $\mu_v = 5.0 \times 10^{-10}\text{m}^2\text{S}^{-1}\Omega^{-1}$, $P = 10$, $V_{ON} = 0.01\text{ V}$, $V_{OFF} = -0.01\text{ V}$, $I_{OFF} = 5.0 \times 10^{-5}$, $I_0 = 1.0 \times 10^{-6}$, $I_{ON} = 1$.

The function of rate variation module is the same as time delay module. As shown in Fig. 10(b), the signal needed to be stored indicates that the processes of learning are completed. Only when message notification signal but not happy message (bad message) is applied, rate variation module will output signals. Hence, we also add three logic gates. This module provides signal in next pro-

cess of learning. Obviously, the time of storage is longer than time delay module. In order to make the memristance of memristor increase slowly in this module, $I_{on} = 6$ of memristor is selected. $R_3 = 700(\Omega)$ is modified. Two resistor $R_1 = 1\text{ k}$ and $R_2 = 500$ are added to adjust the output signal of this rate variation module. The rest of circuit structure and parameters are same to the time delay module. V_{in1} is a signal which indicates that the processes of learning have been finished. V_{in2} and V_{in3} represent input signal of message notification neuron and good message neuron respectively.

3.5. Whole circuit design

Fig. 11 is the whole circuit structure of emotion model with associative memory. The associative memories of good message and bad message are the same, so, for simplicity, we only use the good message for explanation. When message notification is merely applied, because of the large memristance of memristor, the output of synapse is lower than threshold of output neuron, there is no output of HN. But the output signal of MN is stored in time delay module. When the GM signal comes next time, time delay module will output a signal. Through analog subtracter, this signal becomes a negative voltage. This voltage will make the memristance decrease. Due to the existence of ABM, this negative voltage does not have any influence on output neuron. When the message notification comes alone next time, if memristance decreases to a certain value, the output signal of synapse will exceed the threshold of HN. People express happy mood. This process indicates the associative memory has been learned. The output signal of synapse will be stored in rate variation module. When the next process of learning comes, the rate variation module will output a signal and pass it to synapse. The absolute value of this signal is smaller than that outputted by time delay module. This signal is the input of analog adder(positive value). The absolute value of voltage applied to synapse (negative value) is smaller than the voltage which is provided by time delay module(negative value) only. Through analysis of Fig. 3, we can draw a conclusion, under this small voltage, change speed of memristance is faster

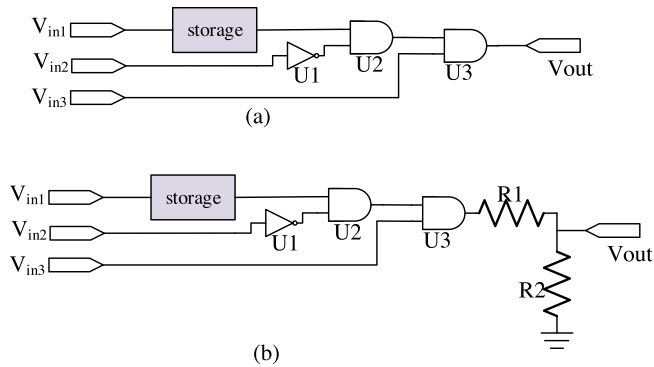


Fig. 10. Time delay module and rate variation module.

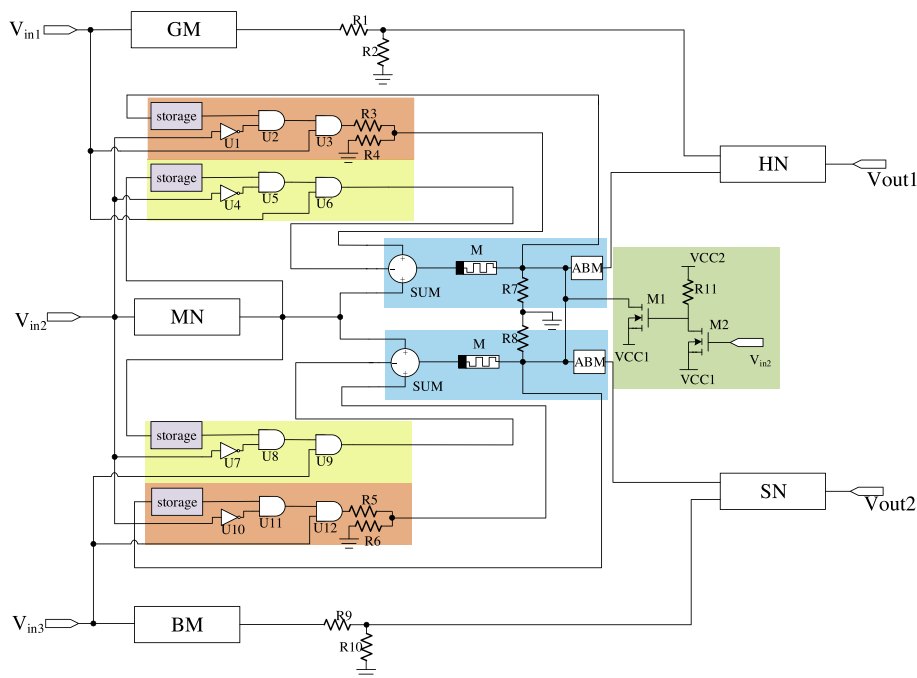


Fig. 11. Whole circuit structure.

than first learning. If only message notification is applied for a long time, output voltage of MN will make memristance increase, that is to say, the associative memory which is formed before will fade away. This is one of the three forgetting processes. When only good message is received or neither good message nor message notification is received, voltage applied to negative electrode of memristor will be almost zero. The module marked by green shade works. (In this module R11 is 1 k(Ω), VCC1 and VCC2 are -1 V and 2 V respectively). This module will provide a voltage of -1 V to the positive

electrode of memristor. In this situation, the memristance of memristor will increase. This is how the other two forgetting processes work.

4. Result analysis

Simulation results are shown in Fig. 12. Process A and B are the associative memories of good message and bad message respectively. For process A. At first, only good message can cause an out-

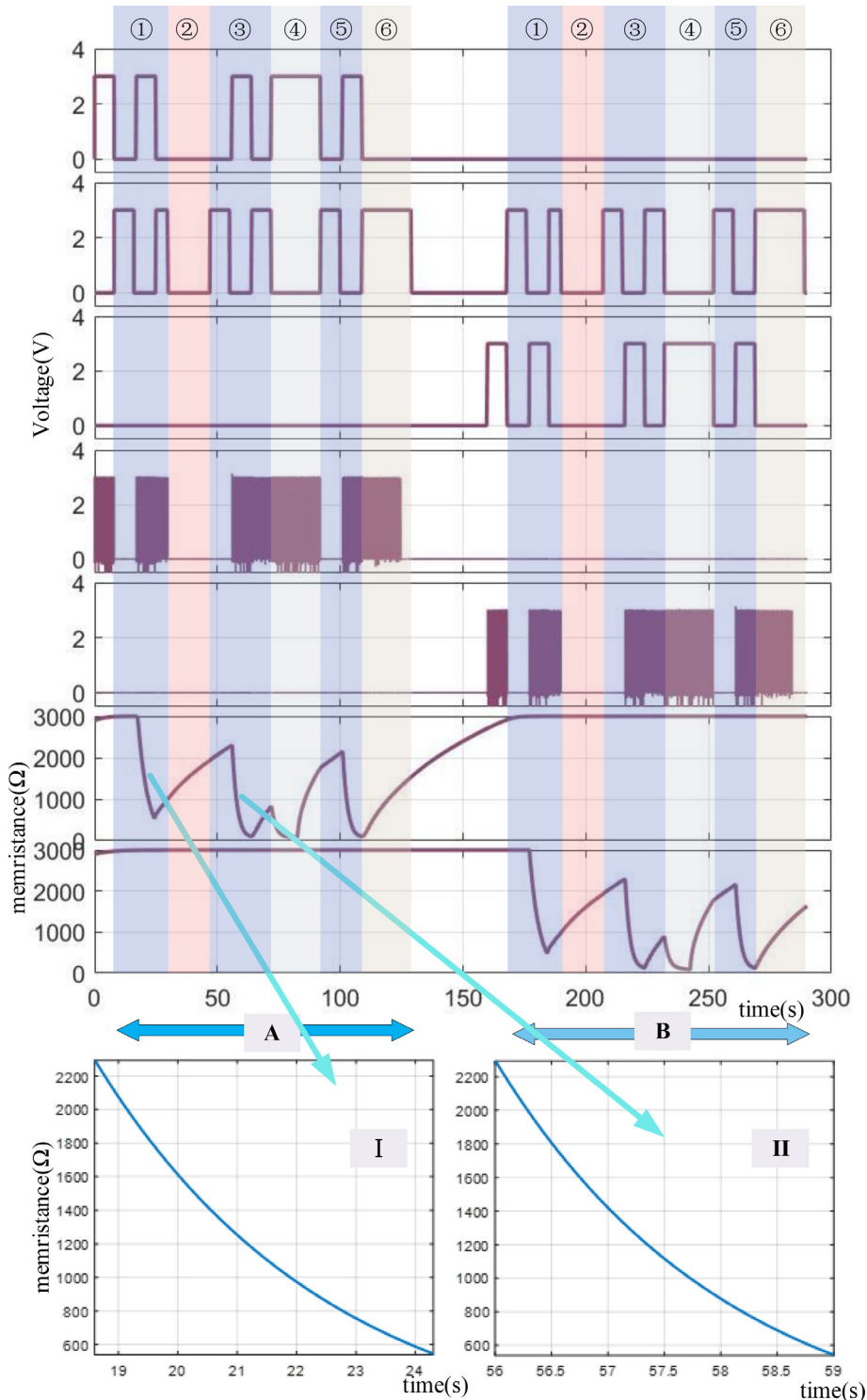


Fig. 12. Simulation result of emotion model with associative memory (a) good message (b) message notification (c) bad message (d) happy neuron (e) sad neuron (f) memristance of the first synapse (g) memristance of the second synapse.

Table 2
Comparison with previous works

Work	Learning	Forgetting 1	Forgetting 2	Forgetting 3	Variable learning rate	Time delay	variable learning rate with time delay
[28]	✓	×	×	✓	×	×	×
[30]	✓	×	×	✓	×	×	×
[29]	✓	✓	✓	✓	✓	×	×
This work	✓	✓	✓	✓	✓	✓	✓

put pulse of happy neuron (HN), and message notification can not. Test① is the first process of learning, good message comes behind message notification. And then, only message notification is applied, there is an output pulse of HN. That is to say, associative memory is completed. Test② is a process of forgetting, neither good message nor message notification is applied. And next time, when message notification comes only, there is no output signal of HN. Test③ is the second process of learning. Analysis is the same as the first learning. Test④ is another forgetting, only good message is applied for a while. And then notification comes only, there is no output signal of HN. Test⑤ is the third process of learning. Analysis is the same to the first learning. Test⑥ is the last process of forgetting, only message notification is applied for a while, we can see that the output pulse of happy neuron vanishes at end of this process. Pictures I and II are the enlargements of memristance change during the first and second learning respectively. In these two pictures, we control changes of memristance to be the same to each other. Through observing the length of time consumed, we can know the speed of the second learning is faster than the first learning. That is to say, the learning rate is variable. After process A, we do not receive any message. The associative memory between good message and message notification has vanished completely. Process B shows the associative memory between bad message and message notification. The analysis of process B is the same as process A. So, we can draw a conclusion, this circuit can realize the function of emotion model with associative memory well.

Remark: As is shown in Table 2, the difference between our article and previous works is demonstrated. A model for modeling the affections was proposed in [28], but this paper only implemented the associative memory and the processes of forgetting. Paper [30] used memristive circuit to simulate the learning and forgetting processes of emotions. In [29], the three processes of forgetting and the variable rates of learning were realized in emotion model. But they did not consider the variable learning rates with time delay. In this article, we realize this useful function. When the time delay is exist, the learning rate can also be variable.

5. Conclusion

In this article, an emotion model with associative memory is realized through a memristance circuit. Comparing to the previous works, the variable learning rate with time delay can be realized. This more ordinary situation can be used to simulate the emotional changes when we check the messages after SMS ringtone is received. At first, the SMS ringtone will not cause any emotional fluctuations. We will feel happy or sad based on whether the message is good or bad after the SMS ringtone is received. This learning process gradually forms a connection between SMS ringtone and different moods. Next time, when the SMS ringtone comes, we will feel happy or sad. We also consider three processes of forgetting: only when good (bad) message is applied, only when message notification is applied and neither good (bad) message nor message notification is applied. After the forgetting processes, the bond

between SMS ringtone and different moods will disappear. When the SMS ringtone acts alone, we will not feel happy or sad. If another learning process is appended after one round of forgetting process, the learning rate will actually get higher than before. All works finished in this article will provide an option for future emotional learning. These functions presented in this paper will help the emotion robot gain stronger emotion learning ability. However, some improvements need to be finished in the future. Firstly, the variable speed of forgetting is one of the problems that need to be considered in future research. Secondly, when the bond between good mood and message ringtone is built, if we directly connect bad mood and the ringtone without putting it through forgetting process, both emotions (being happy and being sad) will show up if the message ringtone rings, which is definitely not to be expected and needed to be fixed someday.

CRedit authorship contribution statement

Linmao Yang: Methodology, Validation, Investigation, Writing - original draft, Writing - review & editing. **Chunhua Wang:** Conceptualization, Resources, Writing - review & editing, Supervision, Project administration, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Chunhua Wang received the M.S. degree from Zhengzhou University, Zhengzhou, China, in 1994, and the Ph.D. degree from Beijing University of Technology, Beijing, China, in 2003. He is currently a Professor of College of Information Science and Engineering, Hunan University, Changsha, China. He is a Doctor tutor, Director of Advanced Communication Technology Key Laboratory of Hunan Universities, a member of Academic Committee of Hunan University, a Director of Chaos and Nonlinear Circuit Professional Committee of Circuit and System Branch of China Electronic Society. Now, his research interests include memristor circuit, complex networks, chaotic circuit, chaos secure communication, current-mode circuit and neural networks based on memristor. He has presided over 8 national and provincial projects, and published more than 120 papers, among which more than 100 were retrieved by SCI.



Linmao Yang received the B.E. degree from the College of Information Science and Engineering, Hunan University, Changsha, China, in 2019. He is currently pursuing the M.E. degree in the College of Information Science and Engineering, Hunan University, Changsha, China. His main research direction is memristor-based associative memory in the artificial neural network.